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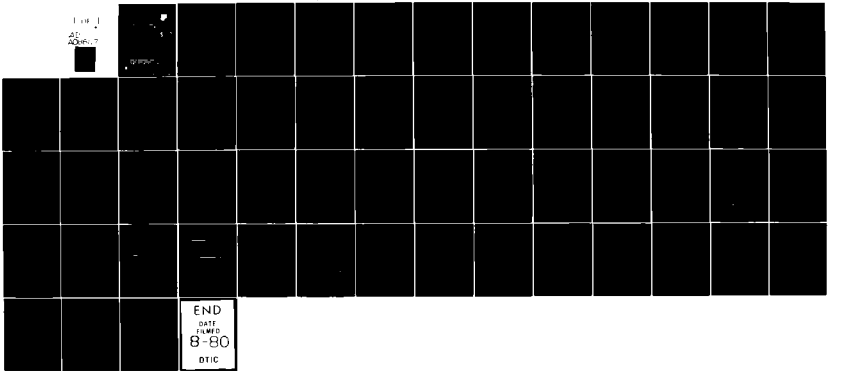

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Interim Report
February 1980

LEVEL II

INVESTIGATION OF OPERATION OF SILICON CCD DELAY LINES

Raytheon Company

Arthur M. Cappon
Wolfgang M. Feist
Edwin G. Goodell
Jay P. Sage

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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*
Theoretical analysis of input/output circuit operation for high frequency CCDs has been completed and a computer program for the analysis of various input/output schemes has been written. Initial analysis shows that the potential equilibrium method, when operated at high speeds, will cause a residual charge to remain in "zero" wells - essentially introducing an unintentional fat zero. This effort primarily reduces the available dynamic range; even at a .5 nanosecond equilibration time only a 1 to 2 percent nonlinearity is introduced.
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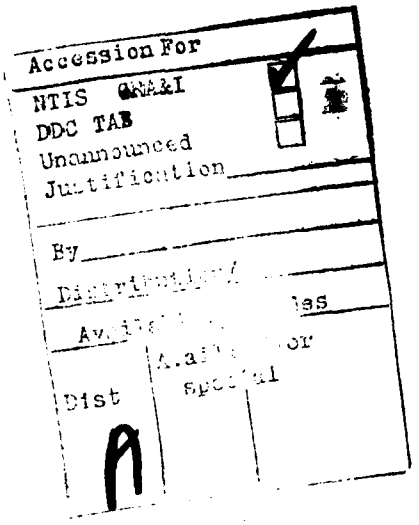
In 2.5 to 4 nanoseconds excess noise in this process is reduced to the thermal noise level. Chip design for the high speed CCD delay line is finished and masks are being fabricated. In addition to the 256 bit delay line with the Raytheon proposed ECMOS (Etched Channel MOS) I/O, the chip contains test structures of 64 stage delay lines, with different ratios of storage to transfer cell length; and both ECMOS and conventional MOS clock drivers.



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SUMMARY

The objectives of this program include the analysis, design, fabrication, evaluation and delivery of high speed charge coupled delay lines.

While buried channel CCD delay lines are known to be theoretically capable of operating at clock rates well in excess of 100 MHz, the practical use of CCDs at high clock rates has been found to be seriously hampered by peripheral limitations. Problems have been encountered in introducing input signals to the CCDs, recovering them after they are transported, and in driving the clock lines at the high clock rates required.

This report begins with a description of the theory of operation and the approach being used for a computer analysis now underway of the input/output characteristics of CCDs operating at high speed. Some of the first results of that study are presented along with conclusions.

The ECMOS transistor structure is then described along with characteristics of experimental devices with performance parameters that are quite promising for use in high speed CCD peripheral circuitry.

A high speed CCD test mask series is being designed under this contract which will incorporate high speed CCD delay lines and input and output test structures along with high frequency amplifier and clock pulse driver circuitry. The mask design of a portion of this new mask series is also discussed.

Plans for the next reporting period are also described.

1. INTRODUCTION

This report describes the work performed and in progress under USAF contract No. F19628-78-C-0167 entitled "Investigation of Silicon CCD Delay Lines." The primary objectives of the contract include the analysis, design, and development of advanced CCDs with input and output circuitry as well as delay stages capable of operation at 100 MHz and above clock frequency.

A high speed 256 stage CCD delay line with high frequency input and output circuits will be developed, and twenty best effort samples will be delivered at the end of the contract.

In addition, the design parameters will be developed for a 1024 stage CCD with monolithic high speed input, output and on-chip clock drivers capable of operating at high frequencies ($f_c \geq 100$ MHz).

The device, circuit and process designs adopted will emphasize future growth potential such that performance characteristics may be extended to much higher operating frequencies in the future.

Contract work for the past reporting periods first emphasized device development and analysis and now concentrates on the design of masks for a test mask series that will be used to evaluate the design tradeoffs of experimental structures. The discussion which follows will describe this work in detail.

2. THEORETICAL ANALYSIS OF CCD INPUT/OUTPUT STRUCTURES

2.1 Purpose and Basic Approach

Considerable effort has been devoted in the past to theoretical analysis of the transport of charge from gate to gate in the main channel of a CCD. Relatively little effort has been applied to a theoretical evaluation of charge flow limitations in the input and output structures in which conversions are made between external signals and charge in the CCD. Some of the results of the charge transfer efficiency studies can be carried over, but there are significant differences.

Since the effects of charge transfer loss accumulate over hundreds or even thousands of transfers, residual charges in the order of 10^{-3}, 10^{-4}, or 10^{-5} are of interest and concern. The I/O structures typically occur only once, and errors do not accumulate. Charge residues affect primarily only the linearity and secondarily, as will be seen later, the noise level of the conversions. Buried channel and short gate structures appropriate to very high speed CCDs have intrinsic nonlinearities of a few percent to begin with, and thus charge residues in the orders 10^{-1} and 10^{-2} are of interest in an analysis of I/O performance.

Another significant difference is that the transfer of charge from one gate to the next has a relatively simple formulation with boundary conditions that permit closed-form mathematical expressions to be found for special cases. The input/output structures and processes are more complex. Numerical analysis is therefore the primary tool for solving the equations, although the results of the numerical analyses may suggest simpler and useful ad hoc models.

The theoretical problem posed by the real CCD I/O structures is far too complex for practical solution even by numerical means. A high speed buried channel structure must be treated in at least two dimensions, and the time required to design and run such a computer program would be very great. Even then the relation of the solutions to the laboratory performance

of devices would be questionable because the actual dopant distributions in multiply-implanted and oxidized structures is not well known. The only way to get reliable specific results is by experimental measurement. The purpose of any theoretical analysis should, therefore, be to gain general insight into the physical factors that limit performance and on their general dependence on the dimensions and other design variables of the structure. This kind of information is useful in arriving at intelligent design choices and in suggesting experimental measurement approaches.

Since the real problem is far too complex to analyze practically, we will develop an admittedly oversimplified model that is easy to formulate as a computer program and requires only modest computation time. The results will not be a quantitatively accurate description of the real CCD, but they will show trends that can be expected to be reliable as design parameters and techniques of operation are varied.

2.2 Formulation of Problem

2.2.1 General Formulation

We will begin with a more-or-less complete and general formulation of the charge flow problem and then systematically introduce the series of approximations that leads to our final model.

The effects of electrostatic fields and carrier diffusion can be handled together using the Fermi potential function;

$$\phi_f = V - V_{th} \ln(n/n_o) \qquad (1)$$

where V is the actual electrostatic potential, V_{th} the thermal voltage KT/q_e, n the density of carriers (electrons), and no an arbitrary constant, conveniently chosen in some cases to be the intrinsic carrier concentration $n_i = 1.5 \times 10^{10} cm^{-3}$. In our analysis we will ignore minority carriers, since in all cases of interest n is much greater than n_i and p.

From the Fermi potential we derive the effective electric field acting on the carriers.

$$\vec{\varepsilon} = -\vec{\nabla}\phi_f \tag{2}$$

The velocity of the carriers is then given as;

$$\vec{v} = -\mu\vec{\varepsilon} \tag{3}$$

This can be taken as the definition of the net mobility μ. In practice, the relation between v and ε is not linear, especially at high field strengths in the range of 1 V/μm. Figure 1 shows experimental values of the net mobility μ_{net} and incremental mobility μ_{incr} for high-quality silicon.

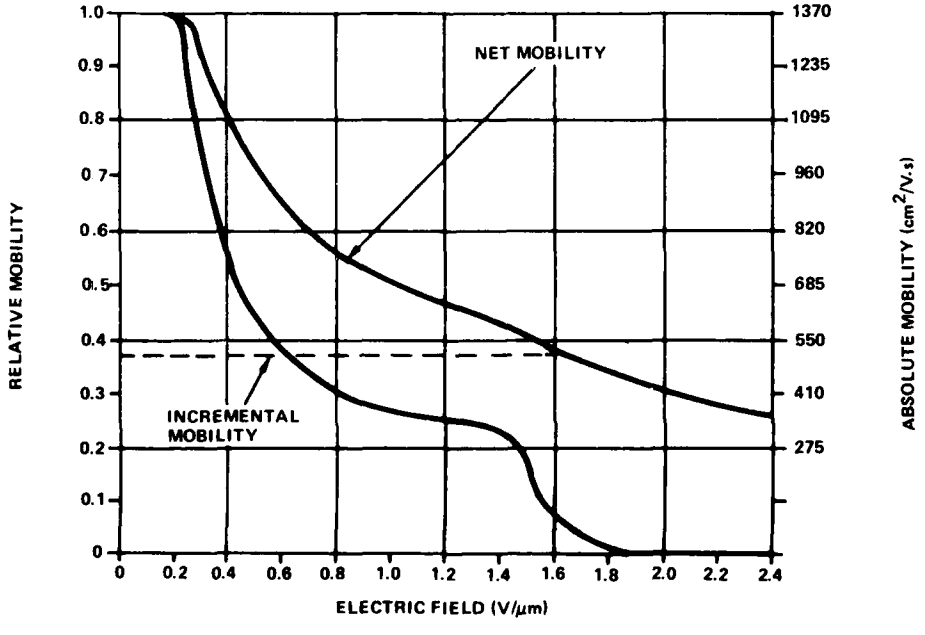


Figure 1. Electric Field versus Mobility in Silicon

$$\mu_{net} = \frac{v}{\varepsilon} \tag{4a}$$

$$\mu_{incr} = \frac{dv}{d\varepsilon} \tag{4b}$$

Note that the net mobility which appears in our equations, falls off more gradually than the incremental mobility. Moreover, in silicon with a low-field mobility of 500 cm^2/v-sec, as is more common in CCDs, the curve probably would look like the dashed curve in Figure 1. As will be seen in Subsection 3.1 later, when we have very short effective gate lengths (~ 1μm), we must begin to consider the effect of mobility reduction.

From the carrier velocity given in Equation (3), we derive the flux of carriers $\vec{F}$ as follows:

$$\vec{F} = n\vec{v} = -n\mu\vec{\varepsilon} = n\mu\vec{\nabla}\phi_f \tag{5}$$

The continuity equation expresses the fact that if no carriers are spontaneously generated (a reasonable assumption over the short time intervals under consideration here), the change in carrier density is the negative divergence of the flow; that is,

$$\frac{\partial n}{\partial t} = -\vec{\nabla}.\vec{F} = -\vec{\nabla}.\ (\mu n\vec{\nabla}\phi_f) \tag{6a}$$

$$= -\mu\vec{\nabla}.n\vec{\nabla}\phi_f \tag{6b}$$

Equation (6b) holds when μ is constant, as we will assume from this point on. Equation (6a) is fairly generally valid. One significant assumption not yet

stated explicitly is that electrodynamic effects are ignored. These include radiation of electromagnetic fields from accelerated charges and magnetic fields induced by time-varying electric fields.

2.2.2 Approximations and Simplifications

2.2.2.1 Limitation to One Dimension

Our first major simplification is to treat all the variables as a function only of the dimension parallel to the direction of charge transport in the CCD channel, which we will call the X-axis. Distributions of carriers into the depth of the structure will be integrated into an effective area concentration. These concentrations will be assumed not to vary across the width of the device. Since the width will typically be 50 μm while the gate lengths and channel depths will be 5 μm or less, this approximation is quite reasonable. Carrier motion in the depth direction will be neglected.

Equations (2) through (6) now take on the form:

$$\frac{\partial n}{\partial t} = -\frac{\partial}{\partial x}\left(\mu n \frac{\partial \phi_f}{\partial x}\right) \tag{7a}$$

$$= -\frac{\mu \partial}{\partial x}\left(n \frac{\partial \phi_f}{\partial x}\right) \tag{7b}$$

Inserting the definition of the Fermi potential from Equation (1), we get:

$$\frac{\partial n}{\partial t} = -\frac{\partial}{\partial x}\left(\mu n \frac{\partial v}{\partial x} - \mu V_{th} \frac{\partial n}{\partial x}\right) \tag{8}$$

The first term represents field-driven flow; the second term represents thermal diffusion ($\mu V_{th} = \mu kT/q_e = D_{th}$ by the Einstein relationship).

2.2.2.2 Local Determination of Potential

We will now make the major assumption that the electrostatic potential $V(x, t)$ at a given point x depends only on the value of the carrier density $n(x, t)$ at that point. This is certainly not always true; the potential in general depends on the charge distribution everywhere. For surface channel devices with the signal charge separated from the gates only be a thin oxide of perhaps 0.1 μm and with gates on the order of 10 μm long, the approximation is very good. The approximation becomes less good as the channel becomes more deeply buried (1/2 to 1 μm below the gates) and as the smallest geometrical features of the gates shrink toward 1 μm (Note: It may be possible later in this program to refine this approximation and use an integral expression and the method of images to obtain more accurate results. The principal interest in making such a refinement would be to see the trend it introduces into the speed of charge transfer and equilibration).

The mathematical consequence of this assumption is the expression:

$$\frac{\partial V}{\partial x} = \frac{\partial V_{ch}}{\partial x} + \frac{\partial V}{\partial n}\frac{\partial n}{\partial x} \tag{9}$$

where V_{ch} is the channel potential when $n = 0$. The second term in Equation (9) accounts for the change in potential caused by the local carrier density. Stated another way, the first term represents the fringing electric field from the gates and the second term represents the field due to mutual repulsion of the charged carriers. Putting Equation (9) into Equation (8), we get:

$$\frac{\partial n}{\partial t} = -\frac{\partial}{\partial x}\left\{\mu n \frac{\partial V_{ch}}{\partial x} - \mu\left[V_{th} - n\frac{\partial V}{\partial n}\right]\frac{\partial n}{\partial x}\right\} \tag{10}$$

The term $\mu\left[V_{th} - n\frac{\partial V}{\partial n}\right]$ represents an effective diffusion constant in which the thermal diffusion constant $\mu V_{th} = D_{th}$ is augmented by $\left(\frac{\partial V}{\partial n}\text{ is negative}\right)$ a term proportional to the local carrier concentration.

2.2.2.3 Constant Effective Capacitance

We will now make the relatively minor assumption of a constant effective capacitance in the relationship between V and n. We thus write:

$$V = V_{ch} - \frac{q_e n}{C} \tag{11}$$

and,

$$\frac{\partial V}{\partial n} = - \frac{q_e}{c} \tag{12}$$

This approximation also is very good for surface channel devices where the total effective capacitance is dominated by the voltage-independent oxide capacitance. In a buried channel device, the effective capacitance of a nearly empty channel is significantly smaller than that of a nearly full one. (Perhaps later in this program the general effect of such capacitance variations on the speed of operation can be studied.) One would, on general principles, expect improved performance because the effective diffusion constant at lower carrier concentrations would be larger, and this is when the extra diffusion speed helps the most.

Substituting Equation (12) into Equation (10) we get:

$$\frac{\partial n}{\partial t} = - \frac{\partial}{\partial x} \left\{ \mu n \frac{\partial V_{ch}}{\partial x} - \mu \left[V_{th} + \frac{q_e n}{c} \right] \frac{\partial n}{\partial x} \right\} \tag{13}$$

We can now express the carrier concentrations in terms of the change in channel potential by making the substitution,

$$V_n = \frac{q_e n}{C} \tag{14a}$$

or,

$$n = \frac{C}{q_e} V_n \tag{14b}$$

where we have chosen the symbol V_n to represent the carrier density expressed as an equivalent voltage. Equation (13) can then be converted to a particularly aesthetic form:

$$\frac{\partial}{\partial t} V_n = - \frac{\partial}{\partial x} \left\{ \mu V_n \frac{\partial V_{ch}}{\partial x} - \mu \left[V_{th} + V_n \right] \frac{\partial V_n}{\partial x} \right\} \tag{15}$$

2.2.3 Computer Formulation

We must now convert Equation (15), a second order partial differential equation, to a form suitable for numerical analysis on a digital computer. As with the preceding treatment, we take the simplest and most direct approach. We define the values of V_{ch} and V_n, which we will denote as VCH and VN for the computer variables, on an array of x values spaced by DX. The quantity inside the braces of Equation (15) is the flux. It will be denoted as F and defined on an array of x values midway between the points on which VCH and VN are defined.

The derivatives are replaced by finite differences, and the factor 1/DX is taken outside the braces. Thus we have:

$$F(I+1/2) = MU* \left\{ \left(\frac{VN(I+1)+VN(I)}{2} \right) [VCH(I+1) - VCH(I)] - \left[VTH + \frac{VN(I+1)+VN(I)}{2} \right] [VN(I+1)- VN(I)] \right\} \tag{16}$$

Note that we have used for VN (I+1/2) the average of the values at the two points I and I+1 at which VN is defined. Also, since the computer functions with integral indices only, we actually add 1/2 to the indices of F in Equation (16) and use F(I+1) in place of F(I+1/2). We will continue to use the latter expression here, however, because it makes the relationships of terms clearer.

The solution proceeds as a two step iteration. First, the current values of VN and VCH are used to calculate values of F. Then the values of F are used to get new values for VN using the following Fortran-type equation:

$$VN(I) = VN(I) - \frac{DT}{(DX)^2} \left[F(I+1/2) - F(I-1/2) \right] \qquad (17)$$

where DT is the time increment for each step of the iteration. Note that the equation has a scaling factor (DT/DX^2). This means that as long as the original differential equation remains valid, reducing all distances by a factor of two results in an identical solution evolving four times faster in time. Relative changes in the mobility also can be extracted as part of the scale factor so that doubling the mobility again results in an identical solution but one that evolves two times faster in time.

Boundary conditions must be provided at the first and last points. The specific choice will depend on the problem, but there are two common types. One occurs when the problem area terminates with a high, steep potential barrier. We can represent this case by requiring that the flux F at the boundary be zero. The second common boundary condition occurs when the problem area terminates with a deep, steep potential well. This case is commonly represented by requiring that VN be zero at the boundary. In our formulation of the problem, the boundaries occur between values of VN and at values of F. We therefore handle this case by setting the first value of VN outside the problem area to zero and writing the boundary value of the flux following Equation (16) as shown in Equation (18).

$$F(\text{boundary}) = MU* \left[VTH+1/2 \; VN(\text{boundary}) \right] *VN(\text{boundary}) \qquad (18)$$

2.3 Cases Analyzed

Actually getting the computer program written, debugged, and running well was more difficult than expected. In particular, although the iterative procedure is quite simple and straightforward, it does not always converge.

Considerable time was required to learn about the problems that could develop in the calculation and to get the program to trap and/or recover from the errors. With DX = 0.2 μm and MU = 500 cm^2/v-sec, time steps no larger than 1/2 psec and some as small as 1 fsec were required to achieve convergence.

The first case that we chose to look at using the computer program was the equilibration phase of the potential equilibration input technique. We chose this case because it is relatively simple (the channel potentials and boundary conditions are constant in time) and because some published results indicate that this input method begins to degrade in the 50 to 100 MHz range. We were curious to see if the computer program would predict a speed improvement using the 1 μm effective gate length of an ECMOS input structure in this case.

The structure of the problem is shown in Figure 2. The source of charge is to the right of the problem area, and the first stage of the CCD is

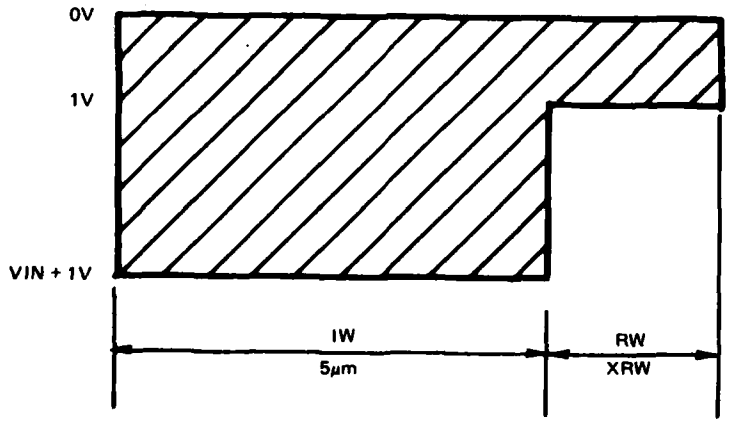


Figure 2. Potential Equilibration Potentials Just Prior to Equilibration

to the left. The problem area iteself contains two regions - an input well (IW) and a reference well (RW). The channel potential in RW is 1 V, and the channel potential in IW is VIN + 1 V, where VIN is a variable input voltage. The input well has a width of 5 μm; the reference region has a variable width XRW. The equilibration phase begins with the entire problem area filled with charge to a Fermi potential of Ov. The left boundary condition is F=0; the right boundary condition is a flux corresponding to zero carrier density just outside the problem area.

2.3.1 Test Case

With VIN=0 we have the classic charge transfer efficiency problem, for which some closed-form mathematical solutions are available. We used this problem as a test case to verify that the numerical iteration procedure was giving plausible results. The self-field-aided diffusion problem, which we simulated by setting VTH=0, has a solution of the form $n(x,t) = n_x(x)n_t(t)$, where the carrier distribution has a shape $n_x(x)$ that does not change in time. The time dependence has the form:

$$\frac{n_t(t)}{n_o} = \frac{1}{1+\left(\frac{t}{\tau}\right)} \tag{19}$$

which can be rearranged to give:

$$\frac{1}{n_t(t)} = \frac{1}{n_o}\left(1+\frac{t}{\tau}\right) \tag{20}$$

To test the constancy of the spatial distribution, we first laid the computer-generated graphs of VN(I)/VN(1) over each other. They were indistinguishable for times of 0.25 nsec or more. As a more sensitive check we compared the ratios of peak charge value VN(1) to the total integrated charge. The values for t=0.5, 1 and 2 nsec agreed to four decimal places; the value at 0.25 nsec differed by 0.1 percent. The results shown

in Figure 3 confirm the theoretical time dependence of Equations (19) and (20). For 0.25 nsec $\leq t \leq$ 2 nsec the maximum deviation in VN(1) was 0.0004 V. The time to make the transition from the square distribution at t=0 to the time-invariant distribution is about 75 psec.

2.3.2 Sample Case

The time evolution of the carrier distribution for a sample case is shown in Figures 4 and 5. Figure 4 shows the distribution of VN; Figure 5 shows the distribution of the Fermi potential with the constant (see Equation (1)) chosen to give ϕ_F=0 at t=0. The length of the reference gate is 5 μm and the value of the input signal 2 V in this case. One sees from these plots that the distribution in the input well is always almost constant. Because of the V_n term in the effective diffusion constant, the effective diffusion in the input well is much larger than that in the reference region. Consequently, the carriers in the input well rearrange rapidly enough to maintain an equipotential distribution.

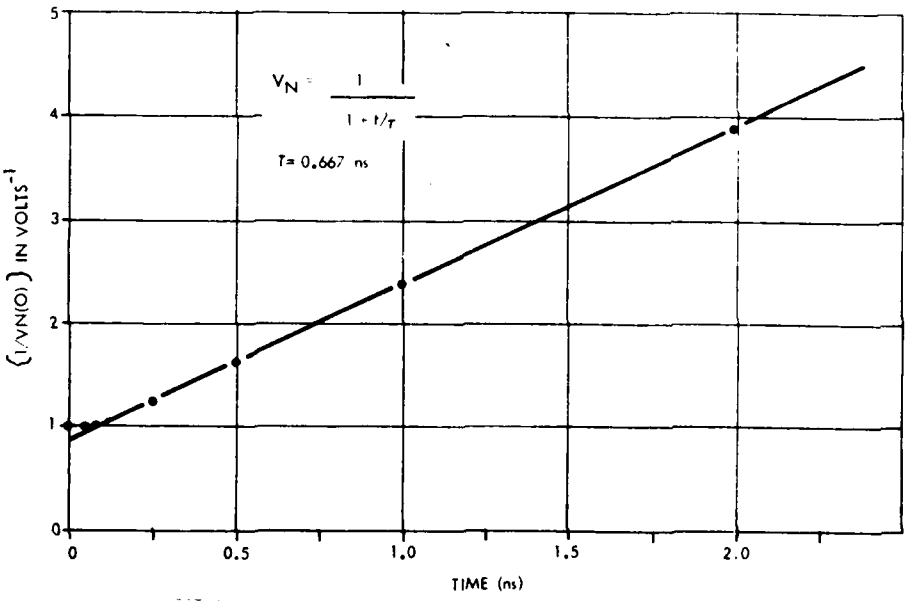


Figure 3. Theoretical Time Dependence of Self-Field-Aided Diffusion

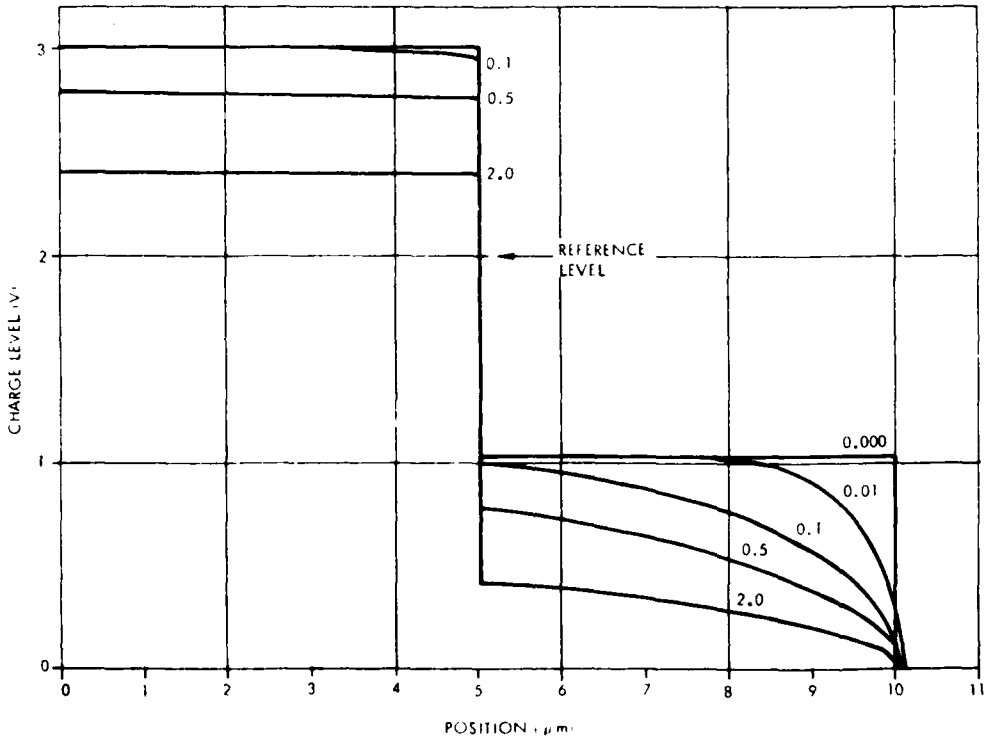


Figure 4. Time Evolution of Charge Level versus Position

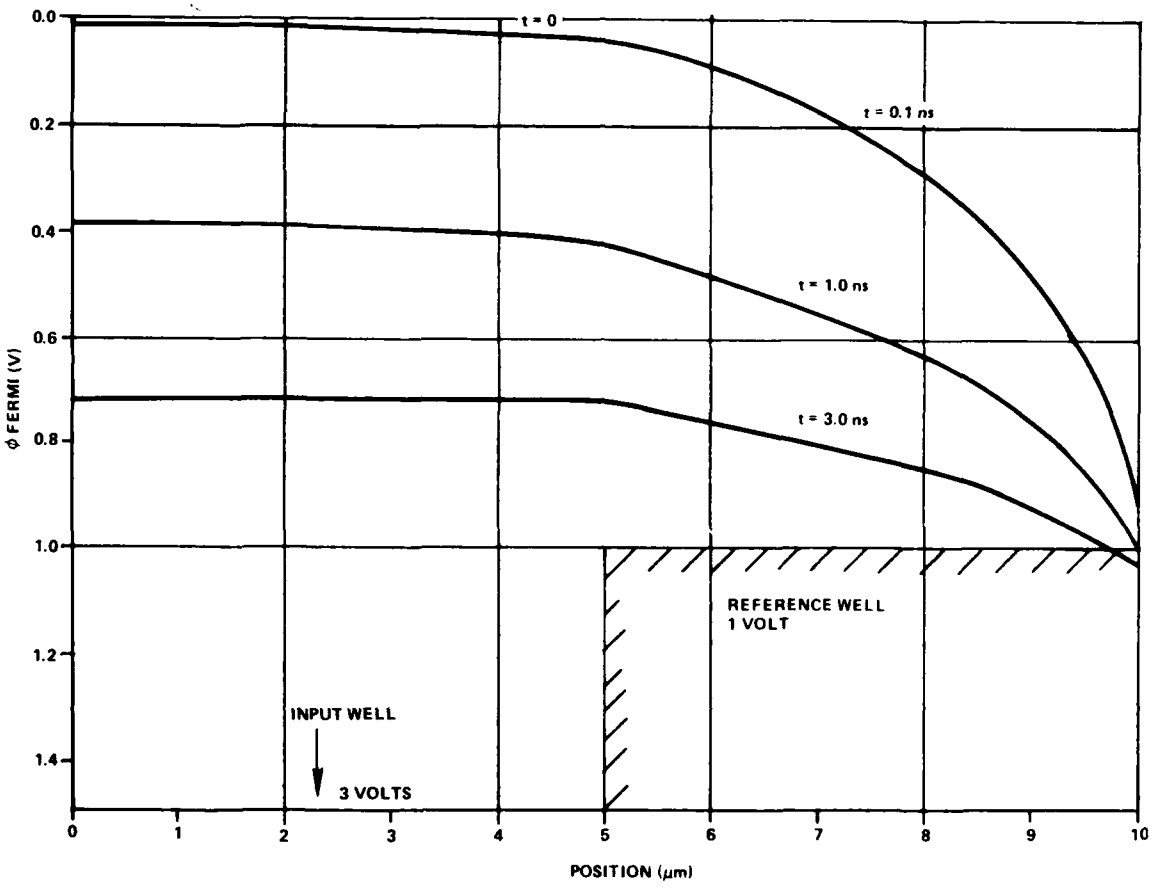


Figure 5. Time Evolution of Fermi Potential versus Position

As a result, for sufficiently large values of VIN (a volt or more, for example), the IW region could be modeled as a single region of width DX with a capacitance that is larger by the ratio XIW/DX, the number of DX intervals in the input region.

2.3.3 General Results

The equilibration phase of the potential equilibration input method was studied for a range of values of VIN and values of XRW of 1, 2 and 5 μm. Figure 6 shows the results for a 1 μm reference gate at four values

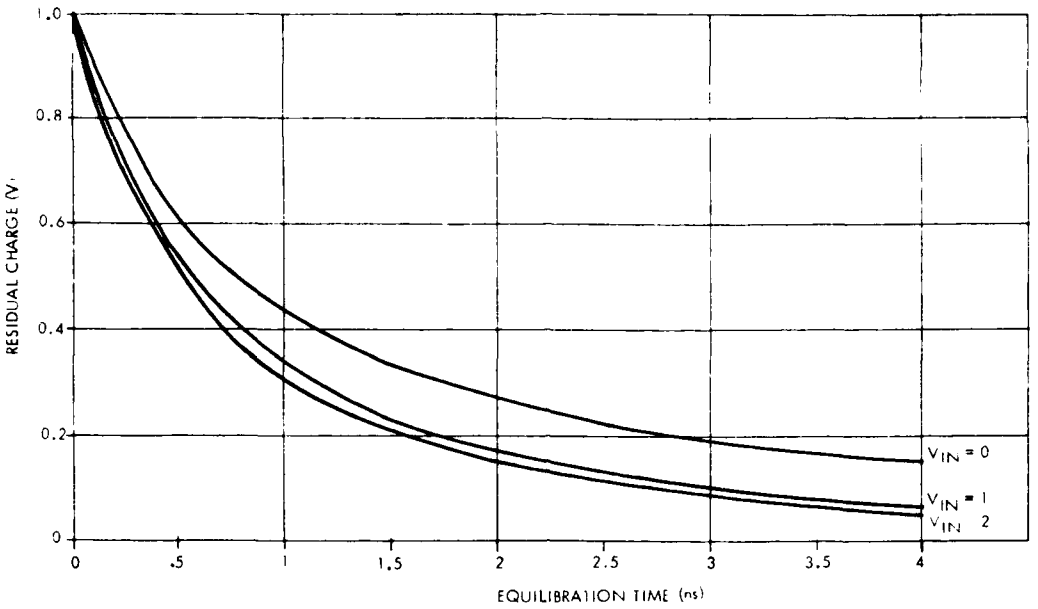


Figure 6. Residual Charge versus Equilibration Time

of VIN, namely VIN=0, 1, 2, and 3 V, for times up to 2.5 nsec. The ordinate shows the amount of charge, expressed in volts, that remains in the input well in excess of the amount that would be there after an infinite equilibration time. Not included in the figure is the excess charge that remains in the reference gate region. When the first stage of the CCD shift register turns on, all of the charge in IW and some of the charge in RW will transfer into the CCD.

The excess charge in the input region above the fully equilibrated value has two effects on the performance of the input. First, it changes the relationship between the input signal and the charge injected into the CCD. It always has the effect of introducing what is commonly called a "fat zero." This means that even when the input signal is set to a value to give zero charge, the actual charge will be larger than zero. This reduces the available dynamic range. In addition, if the excess charge does not depend linearly on VIN, a nonlinearity will be introduced into the voltage-to-charge conversion.

The charge versus voltage relationship derived from Figure 6 is shown in Figure 7 for equilibration times of 0.5 nsec, 1 nsec, 2.5 nsec, and infinity. Only the charge in the input well is included, and it is expressed as the equivalent input voltage for infinite time equilibration. A "least squares straight line" fit reveals that the nonlinearity introduced even at 0.5 nsec is only 1 or 2 percent, not a really significant degradation when one considers that buried channels and fringing effects introduce nonlinearities of this magnitude also.

The second effect of the excess charge on performance is an increase in noise level. When complete equilibration is allowed to occur, only thermal noise is present. Roughly speaking, this results in fluctuations on the order of V_{th} (0.03 V) in the voltage level in the input well. For input signals of 1 V or more, the excess charge has decayed to this level at around 2-1/2 to 4 nsec.

Figure 8 shows results similar to those of Figure 6 but for a reference gate length of 2 μm. Figure 9 shows the result with VIN=2 V for a 5 μm reference gate. The curves all have a similar appearance; only the scale of the time axis is changed. Figure 10 shows the time required to reach a specified residual charge as a function of reference gate length for an input signal of 2 V. Generally speaking, the speed of the equilibration process increases as L^{-1}.

The linear dependence on L may be surprising at first in view of the general L^2 scaling law mentioned in Subsection 2.2.3. This can be clarified as follows. If we compare two structures, one with a 1 μm reference gate and 5 μm input well and another with a 2 μm reference gate and 10 μm input well, the latter will respond four times more slowly. However, if we keep the input well at 5 μm in both cases, there is relatively only half as much charge that must flow across the reference region. This contributes a two-fold speed increase so that the net dependence on length is L rather than L^2.

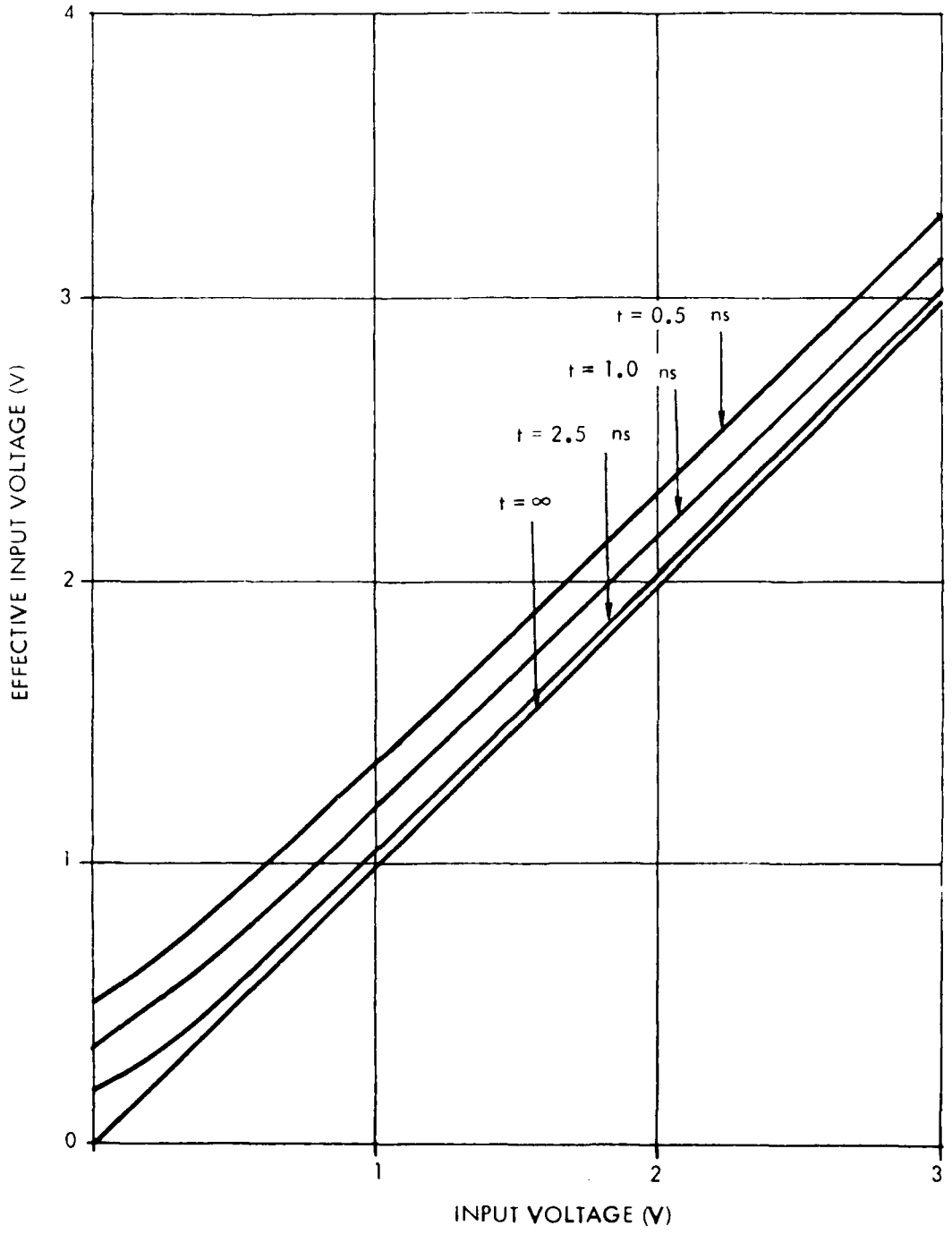


Figure 7. Effective Input Voltage versus Input Voltage

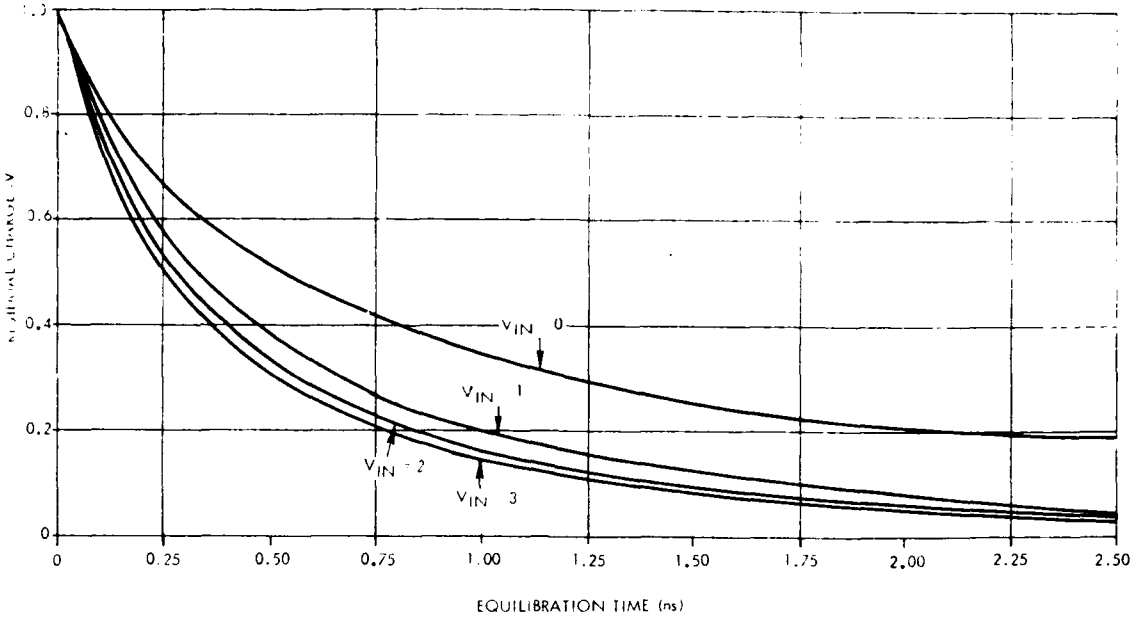


Figure 8. Residual Charge versus Equilibration Time

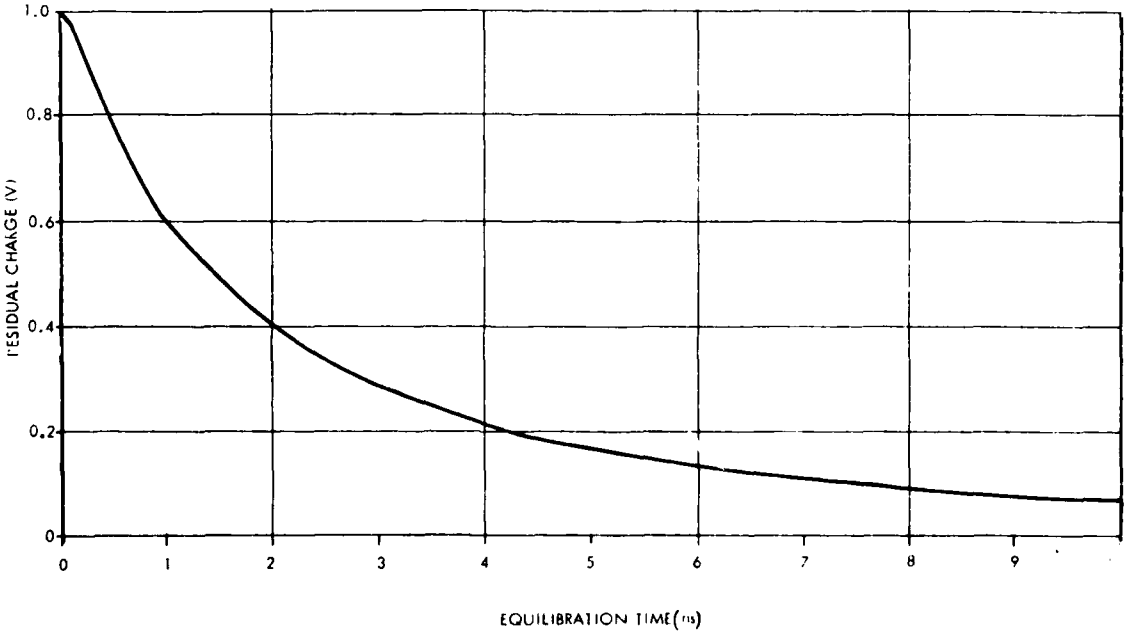


Figure 9. Residual Charge versus Equilibration Time (VIN=2 V)

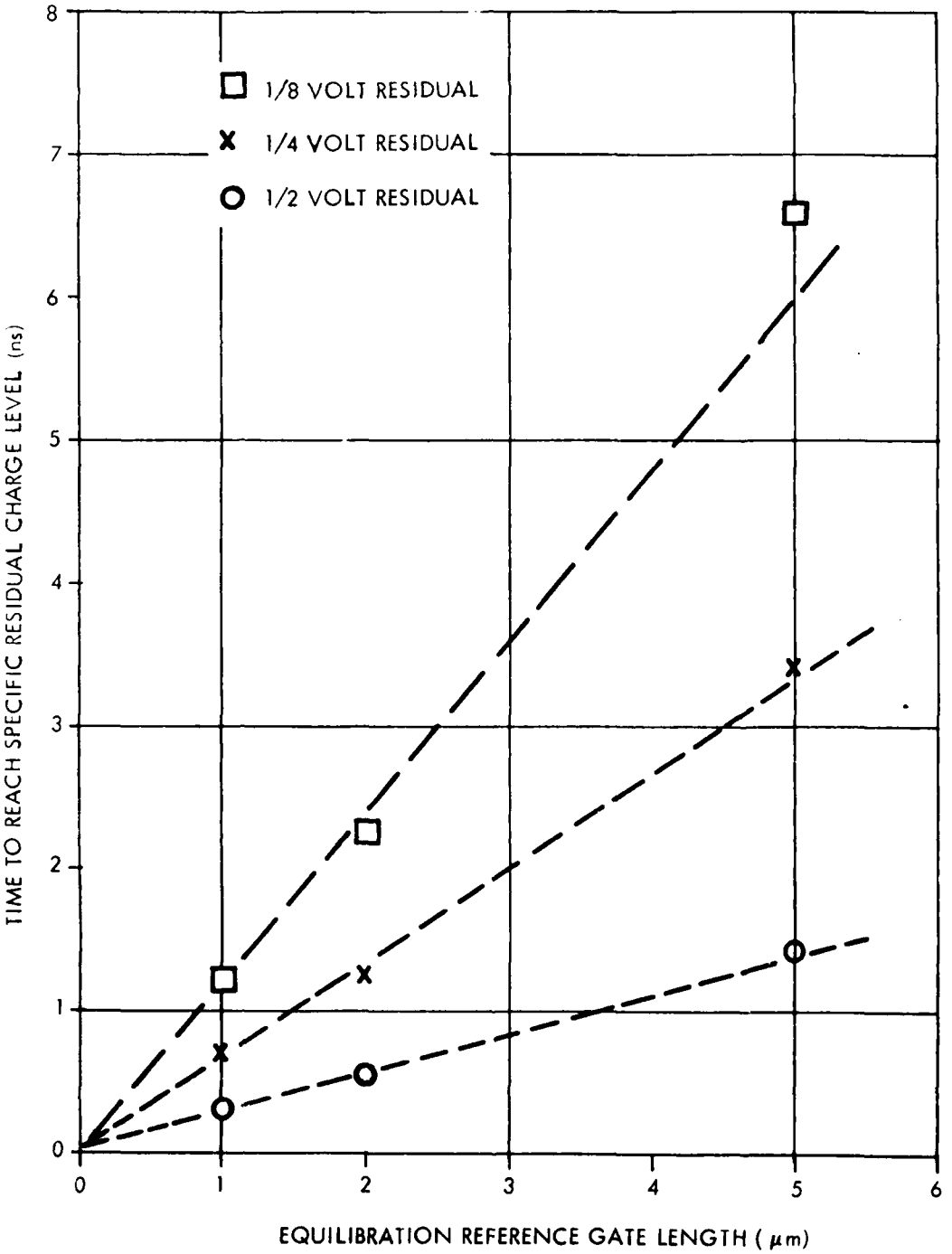


Figure 10. Time to Reach Residual Charge Levels versus Reference Gate Length

We have operated our current high-speed CCD, which has a 7-1/2 μm reference gate and a 15 μm input well, at speeds up to 60 MHz with good results. The scaled gate shrinkage from 7-1/2 to 5 μm should result in approximately a two-fold speed increase (this change scales as L^2). In addition, provided the drift region that is part of the ECMOS structure does not interfere with the operation of the input, the effective shrinking of the reference gate to about 1 μm should provide an additional factor of five speed improvement. The limit could, therefore, be as high as 0.5 GHz.

2.4 Future Theoretical Work

The theoretical work carried out so far has consisted principally of the development of the model and the structure of the computer program. In the next quarter we will examine additional input/output processes and the effects of the approximations used. This work will be described in the subparagraphs below.

2.4.1 Improved ECMOS Equilibration Model

The case of a 1 μm reference gate treated in this report is an incomplete version of the ECMOS input structure. An ECMOS input has a drift region with a deeper channel voltage beyond the effective reference gate, and the input well includes a part which is a floating diffusion. Figure 11 shows the structure which can be compared to Figure 2.

2.4.2 Injection Model

The analysis described above began with an examination of the equilibration phase of the potential equilibration input because this was expected to be the performance-limiting phase. For completeness, the injection phase should also be investigated. The same computer program can be used with only the initial conditions (no charge present) and the boundary condition at the input diode side changed. Both the standard MOS and the ECMOS structure will be considered.

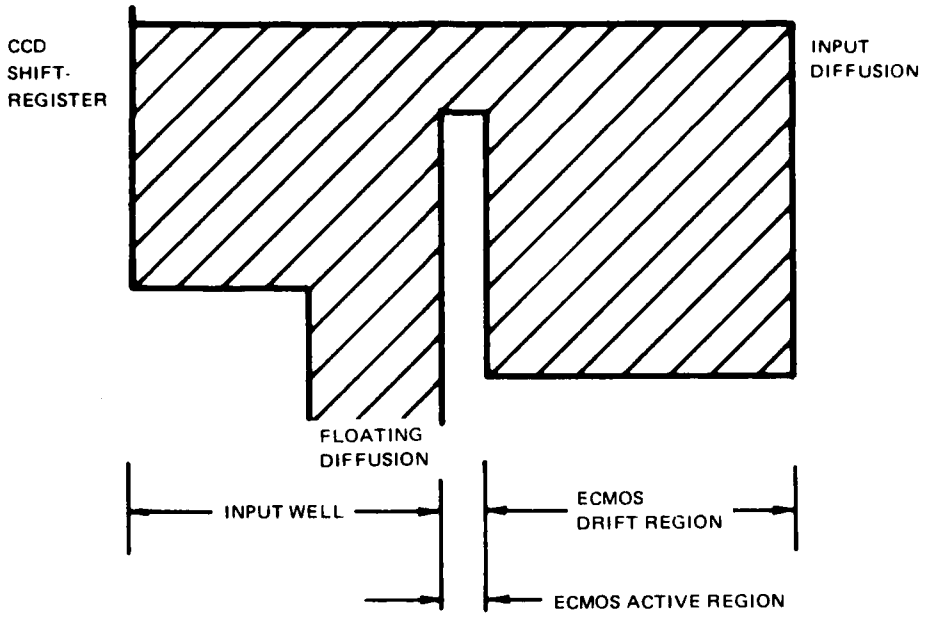


Figure 11. ECMOS Equilibration Structure Potential versus Position

2.4.3 Diode Cutoff Input Model

The diode cutoff technique is expected to be much faster than the potential equilibration technique because the charge is always field-driven. The injection phase is similar to the potential equilibration injection phase. The cutoff phase, however, involves a time-dependent change is the reference gate level from at or below the input well level to above the signal level. The exact way in which the cutoff occurs can be expected to influence the results. Figure 12 shows schematically the kinds of initial, intermediate, and final conditions expected with the standard MOD structure. The ECMOS situation is similar but more complex.

2.4.4 Output Structures

The floating-diffusion output structure can be operated in two ways which are similar to the input techniques. The ECMOS output structure is essentially identical to the input structure; the conventional MOS output

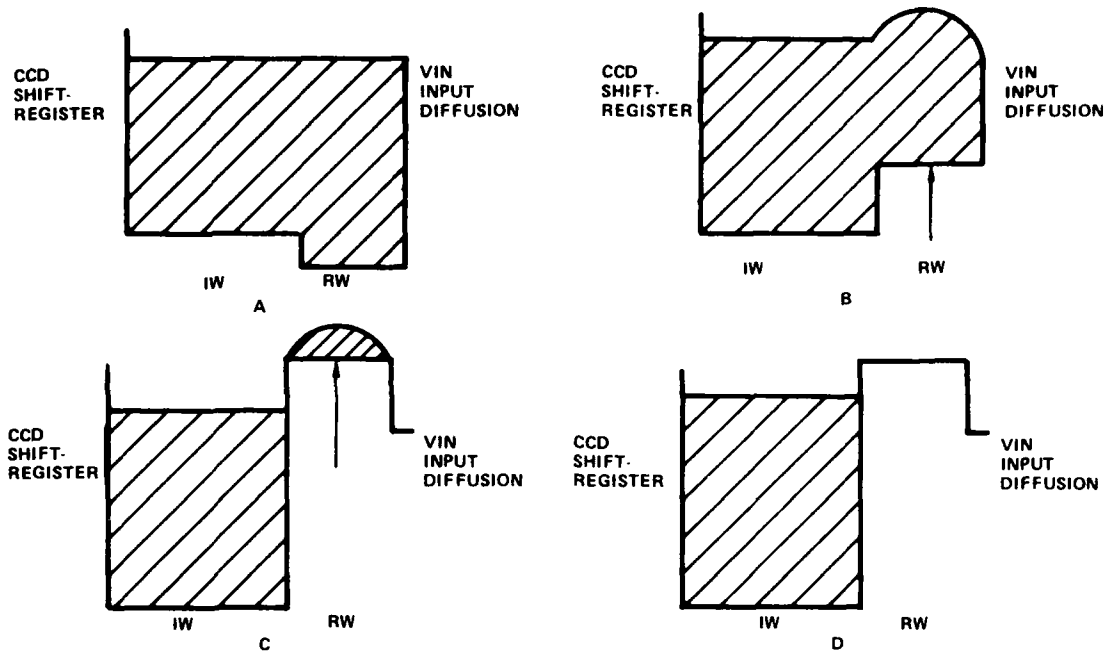


Figure 12. Diode Input Cutoff Method Operating Conditions

structure has, in addition, the floating diffusion, which is not present in the conventional MOS input structure. Consequently, the analysis of the output performance should be straightforward.

2.4.5 Effects of Approximations in the Formulation

A number of rather extreme approximations were used in Subsection 2.2.2 to derive the formulation that will be used for the bulk of the theoretical analysis. Some insight into the effects of these approximations can be achieved by treating some cases more carefully.

The simplest improvement to make is to introduce gradations in the values of the zero-charge channel potentials to represent more accurately the effects of fringing fields from the gates to the buried channel.

The effect of carrier velocity staturation and voltage-dependent capacitance can also be examined in a straightforward manner. The nonlocal dependence of electrostatic potential on charge density can be

simulated by developing the next order of approximation in which the potential depends not only on the local charge density but also on the charge density in the neighboring intervals.

All of these changes will add considerable time to the core computation in the innermost loop. Computer time may become too great to permit exhaustive analyses to be carried out with the more exact formulation, but any significant trends should be revealed from a few key cases.

3. CCD/ECMOS COMPATIBLE TECHNOLOGY

During this phase of the contract, we concentrated our efforts on working out design and processing details for the high speed CCD as well as the ECMOS devices to be used for the CCD input, output, output amplifier, and clock driving devices.

The design and fabrication of the high speed CCD delay line will closely follow the methods successfully used for the Raytheon 60 MHz CCD. The frequency limitations of this device at 60 MHz are primarily due to the output amplifier response. The frequency response limit imposed by the charge transfer properties of the CCD is substantially higher.

The above conclusion was derived from the fact that the output pulse responses for the 64 stage and 128 stage devices looked identical when clocked at 60 MHz. The excellent high frequency performance of these CCDs was obtained in spite of the fact that the gate length was 7.5 μm for the transfer and storage cells, and the fact that the devices were of the two-phase type. In addition, all gate electrodes were made of polysilicon, with electrode overlaps of 1.25 μm. For the purposes of this contract, the channel width of the CCD will be reduced from 225 μm to a value in the range 50-100 μm, and cell electrode lengths will be lowered to 5 μm. The gate electrode overlap of 1.25 μm will be retained. These changes will improve high frequency transfer efficiency and reduce the clock capacitance to be driven. A further modification will be the use of poly Si-Al or TiW-Al instead of polysilicon for the second layer of gate electrodes (storage cell electrodes). The reduced cell electrode lengths will enable us to build a straight 256 stage device with 33 percent shorter overall length.

In the past, our 60 MHz CCDs have been made using an ion implanted guard band to confine the charge to the CCD area in the direction perpendicular to its propagation, and to isolate the transistors of the amplifier from each other. This isolation method uses up more space, requires a separate registration step, and leads to higher oxide steps than the so called coplanar or semirox isolation methods.

In the coplanar method, the device to be isolated is first protected by an oxidation mask made up of SiO_2 and Si_3N_4. The unmasked silicon substrate is etched to a depth about one half the desired field oxide thickness. Boron is then implanted into the surface of the high resistivity p-type silicon to prevent inversion, and field oxide is then grown by thermal oxidation. After this, the masking layer is stripped and the device is formed.

The semirox isolation method is a modification of the coplanar technique which omits the etching of the substrate. As a result, the field oxide forms a step which is approximately one half of its oxide thickness due to the silicon consumed during the thermal oxidation.

The coplanar and semirox isolation methods offer the important advantage that they permit direct contact of field regions to heavily doped regions such as sources and drains of field effect transistors without causing low reverse breakdown voltages. This is not possible with conventional guard band isolation since guard bands are heavily doped and adequate spacing must be provided between them and the source and drain regions.

While ECMOS transistors are readily compatible with the coplanar or semirox isolation, buried channel CCDs using our existing process are not at the present time. While surface channel CCDs have been fabricated at Raytheon with the coplanar isolation which perform as well as guard banded devices, we have not achieved similar results with buried channel CCDs. We believe the phosphorus implant used by us to create the buried channel penetrates the fringe of the isolation region and overcompensates its boron doping. As a consequence, spurious channels have been formed at the boundaries of the CCD buried channels shorting them out.

Although we could correct this situation by increasing the boron dose in the field, this would also reduce the breakdown voltage of the source and drain regions. For this reason, our new high speed CCD test pattern will utilize coplanar isolation for I/O and transistor structures and guard band isolation for the buried channel CCDs.

3.1 ECMOS Transistor Device Development

Although the work described below was not supported by contract funds, this section is included since ECMOS transistors will be used in the High

Speed CCD/ECMOS technology under development. The ECMOS transistor offers the main features of the well known D-MOS and V-MOS transistors, namely a short active channel length (of the order of 1 μm) which does not require precision lithography for its fabrication, and a relatively high drain to source breakdown voltage. The main advantages of ECMOS relative to this contract reside in its excellent threshold control, small gate capacitance, and the compatibility of the fabrication procedure with that of CCDs.

The gate capacitance of ECMOS transistors can be relatively small since the portion of the gate covering the drift region can be separated from the substrate by an oxide which is substantially thicker than the gate oxide.

As with D-MOS and V-MOS transistors, a high drain to source breakdown voltage is achieved by employing a drift region in series with the short channel control regions. The purpose of the drift region is to accommodate the voltage difference between the drain voltage and the voltage which can be supported across the active short channel region without punching through. The punch-through voltage increases with the square root of the p-doping concentration in the short channel region and thus increases with the threshold voltage for a given gate oxide thickness.

In order to obtain optimum performance from such a transistor the electric field in the short channel region should approach 10^4 V/cm. At this electric field strength the carrier velocity starts to saturate and close to the minimum possible transit time is achieved. A higher field strength is not advisable since it will not greatly increase carrier velocity and will aggravate short channel effects (drain-voltage dependence of the threshold voltage, and/or punch-through).

The family of drain characteristics with gate voltage as a parameter can be used to determine whether or not a given device attains optimum carrier velocity. As the drift velocity saturates the transconductance reaches its upper limit and becomes independent of the gate voltage. This can be shown as follows in Equations (21) and (22).

$$I_D = \frac{Q}{T} = Q \frac{v_s}{L} = \frac{\epsilon \epsilon_o}{t} (V_G - V_t) (L) (W) \frac{v_s}{L} \quad (21a)$$

$$I_D = \frac{\epsilon \epsilon_o}{t} (V_G - V_t) (v_s) (W) \quad (21b)$$

$$g_m = \frac{\partial I_D}{\partial V_G} = \left(\frac{\epsilon \epsilon_o}{t}\right) (v_s) (W) \quad (22)$$

where

W = channel width
L = channel length
v_s = saturated drift velocity
T = transit time
Q = charge induced by $V_G - V_t$
V_G = gate voltage
V_t = threshold voltage
t = thickness of gate oxide

Note in Equation (22) the interesting fact that at velocity saturation the drain current and the transconductance do not depend on the channel length, L. However, a channel length shorter than necessary to achieve velocity saturation can still be important for high frequency operation since it affects the transmit time

$$\left(T_{min} = \frac{L}{v_s} = \frac{C_{ox}}{g_m}\right),$$ the gate capacitance $$\left(C_{ox} = \frac{\epsilon \epsilon_o}{t} (W) (L)\right),$$

and the on-resistance of such a device.

The parameters for our ECMOS test structures can be used to determine whether they operate at close to the carrier velocity limit. Using $t = 7 \times 10^{-6}$ cm, $W = 7.5 \times 10^{-3}$ cm and $(g_m)_{max} = 1.8$ m A/V in Equation (22) we obtain a v_s of 4.75×10^6 cm/sec. This is approximately 80 percent of the saturated velocity (6×10^6 cm/sec) available in bulk silicon.

The following requirements apply concerning the drift region:

1) It must conduct sufficiently to permit attainment of an electric field $E_s = 1 \times 10^4$ V/cm in the active channel region
2) It must be capable of carrying the current delivered by the short channel region under optimum conditions

Assuming an average drift velocity, v_d, for the drift region, the second condition implies Equation (23a) which can be as (23b).

$$\frac{\epsilon\epsilon_o}{t} (V_G - V_t) (W) (L) \left(\frac{v_s}{L}\right) = \frac{\epsilon\epsilon_o}{t_d} (V_G - V_{td}) (W) (L_d) \left(\frac{v_d}{L_d}\right) \quad (23a)$$

$$\frac{V_G - V_{td}}{V_G - V_t} = \left(\frac{t_d}{t}\right) \left(\frac{v_s}{v_d}\right) \quad (23b)$$

where

t_d = oxide thickness over the drift region

V_{td} = threshold voltage in the drift region

For practical case one may assume

$$v_d \approx 0.1\, v_s, \text{ and } \frac{t_d}{t} \approx 3$$

therefore

$$V_G - V_{td} \approx 30 (V_G - V_t) \quad (24)$$

Consequently, if we wish to use a gate voltage exceeding V_t by 10 V, (corresponding to $I_D/W = 3A/cm$) the threshold voltage for the drift region must be negative and $V_{td} \approx -300$ V. This corresponds to the charge density shown in Equation (25) which corresponds to a density of electronics charge of $N = 2.4 \times 10^{13}/cm^2$.

$$Q/cm^2 = \frac{\epsilon \epsilon_o}{t_d} V_{td} = \frac{4 \times 8.85 \times 10^{-14}}{2.8 \times 10^{-5}} (300) = 3.8 \times 10^{-6}\,coul/cm^2 \quad (25)$$

The charge density calculated in Equation (25) can be located in the oxide as a positive fixed charge, or, more conveniently, can have the form of a donor implant into the surface of the silicon. For both the value of N is rather high to achieve in practice. More easily attainable conditions require that an N of approximately $0.6 \times 10^{12}/cm^2$ be used which will raise v_d to approximately $0.4\ v_s$.

Assuming a phosphorus implant is used to obtain the above conditions a dose of $6 \times 10^{12}/cm^2$ and a junction depth of 7×10^{-5} cm, the dopant concentration will be in the order of $8.6 \times 10^{16}/cm^3$.

A boron concentration in excess of this value must then be added to provide threshold control in the short-channel region, and to electrically isolate the source of the ECMOS transistor as shown in Figure 15.

Figures 13 through 15 show three different ECMOS transistor structures we are investigating. Structure (Figure 13) will be referred to as type A. It relies on the fixed positive charge contained in the oxide covering the drift region L_D to invert the drift region more strongly than the channel region at low gate voltages. The structure shown in Figure 14 as type B has a phosphorus implant in most of the drift region.

Structure (Figure 15), type C, is the most suitable one of the three for clock driver and output amplifier applications. In this case the phosphorus doping is implanted during the CCD fabrication sequence and before the device areas are formed. It does not require accurate masking since the excess implant is automatically removed when the silicon surface is etched prior to the formation of the coplanar field oxide.

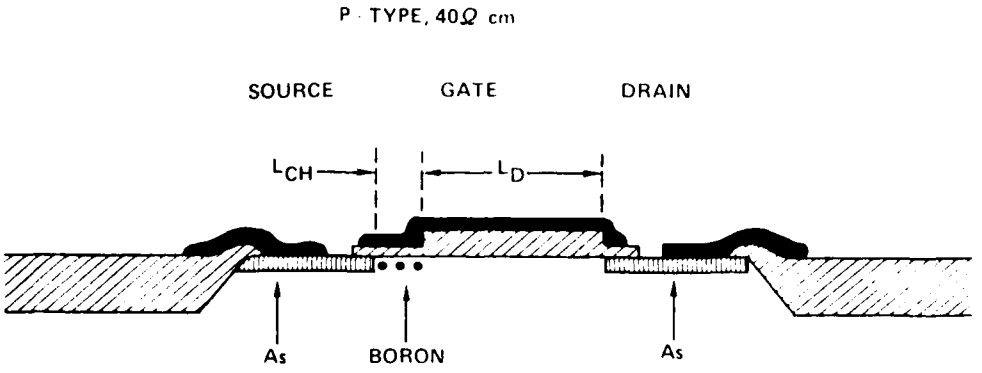


Figure 13. ECMOS Transistor Suitable for Small Gate Voltage Applications

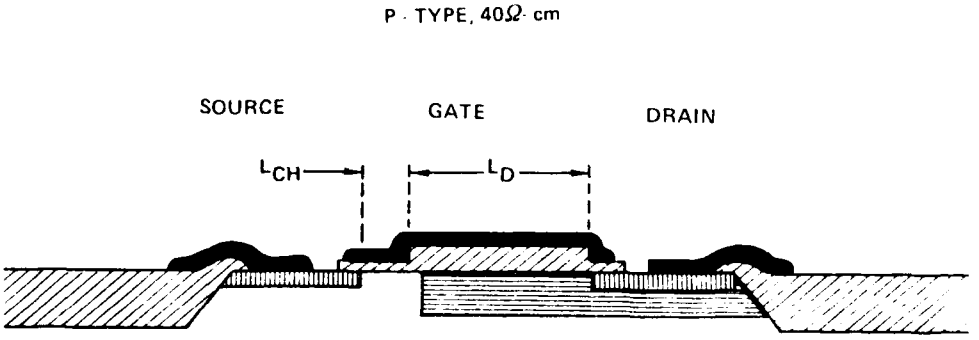


Figure 14. ECMOS Transistor with Reduced On-Resistance Suitable for Large Gate Voltage Applications

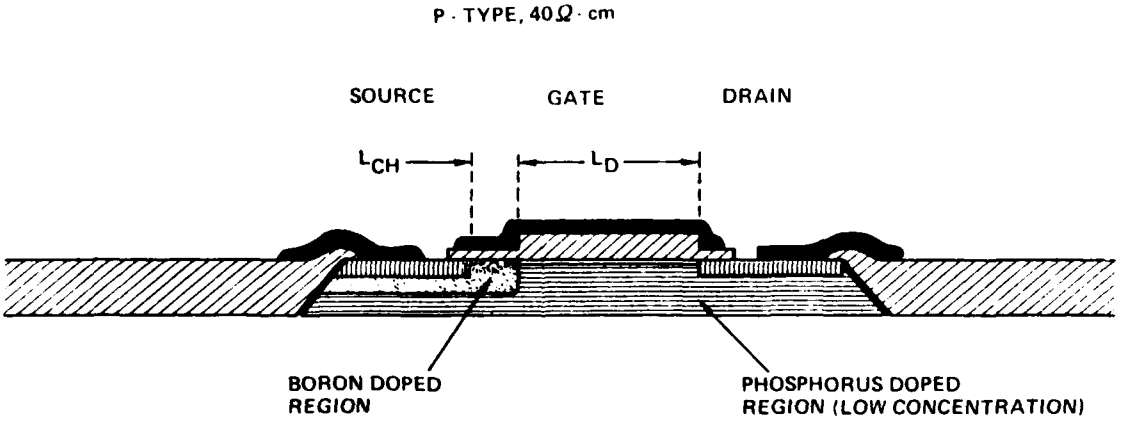


Figure 15. Alternative ECMOS Transistor with Reduced On-Resistance Suitable for Large Gate Voltage Applications

Note that the boron threshold implant serves two functions in the type C structure. It serves to adjust the threshold for the short channel region, and also to diode-isolate the source from the n-type layer. To serve both functions the boron must therefore be driven to a depth exceeding the shallow arsenic-doped source region. Typical S/D families and surface potential v_s gate voltage characteristics are shown in Figures 16 through 18 for the ECMOS structures shown in Figures 13 and 15. In all cases, the length of the short channel section was L = 1 μm, while the width was W = 7.5 μm. For each type of device, the effect of having a drift region of either L_D = 4 μm or L_D = 6.5 μm is also indicated.

As may be expected from the previous discussion, Figures 16 and 17 show a dramatic change in device characteristics with the length of the drift region. When the phosphorus dose is relatively small ($1 \times 10^{12}/cm^2$) and L_D = 6.5 μm the electric field at the short channel region is too small to support a saturated carrier velocity. In contrast for a phosphorus dose of $3 \times 10^{12}/cm^2$, there is much less dependence on L_D since the drift region impedance is much less than that of the short channel region.

3.2 CCD/ECMOS Wafer Fabrication Process Development

The major features of our new CCD fabrication method can be summarized as follows:

1) Ion implantation will be used for most doping steps including isolation, gettering, buried channel, threshold control, and source/drain because of the wide degree of accuracy and reproducibility it affords, as well as the cleanliness it achieves by doping though an oxide and the convenience of using photoresist as an implantation mask.

2) The potential profile for 2 phase buried channel CCDs will be created by the use of two phosphorus implants avoiding the generally used and difficult to control compensation method using phosphorus and boron dopants. In addition, the amount of dopant in the substrate will be minimized.

3) Self aligned gates will be created by doping source and drain regions while they are covered by the gate oxide. Thus, undercutting of the gate oxide under the gate electrodes will be avoided.

4) The polysilicon layer will be doped by phosphorus diffusion since this results in a very low sheet resistance (20 Ω^2 for 5000Å of thickness).

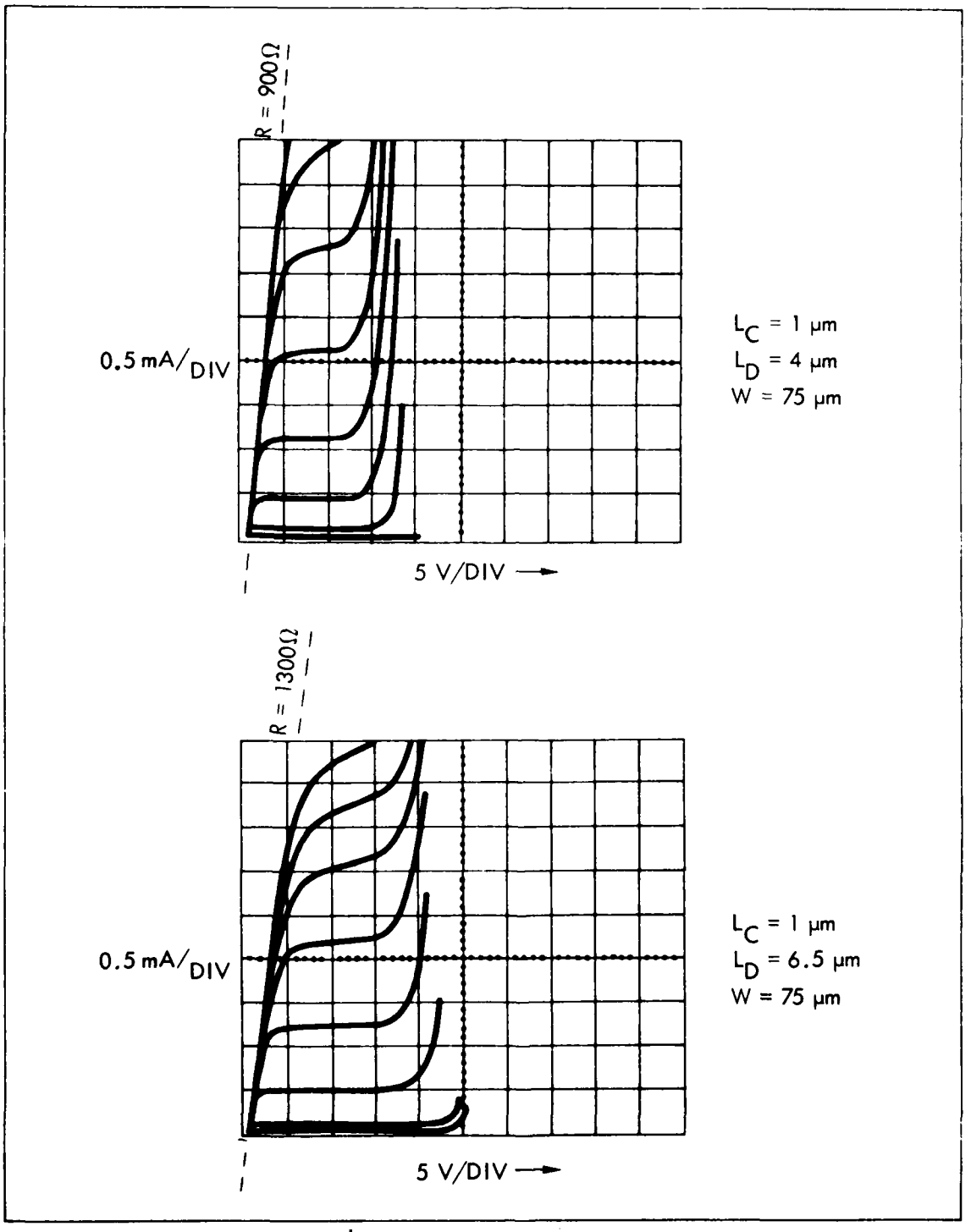


Figure 16. Source/Drain Families of ECMOS Devices (Type A) with L_D of 4 μm and 6.5 μm

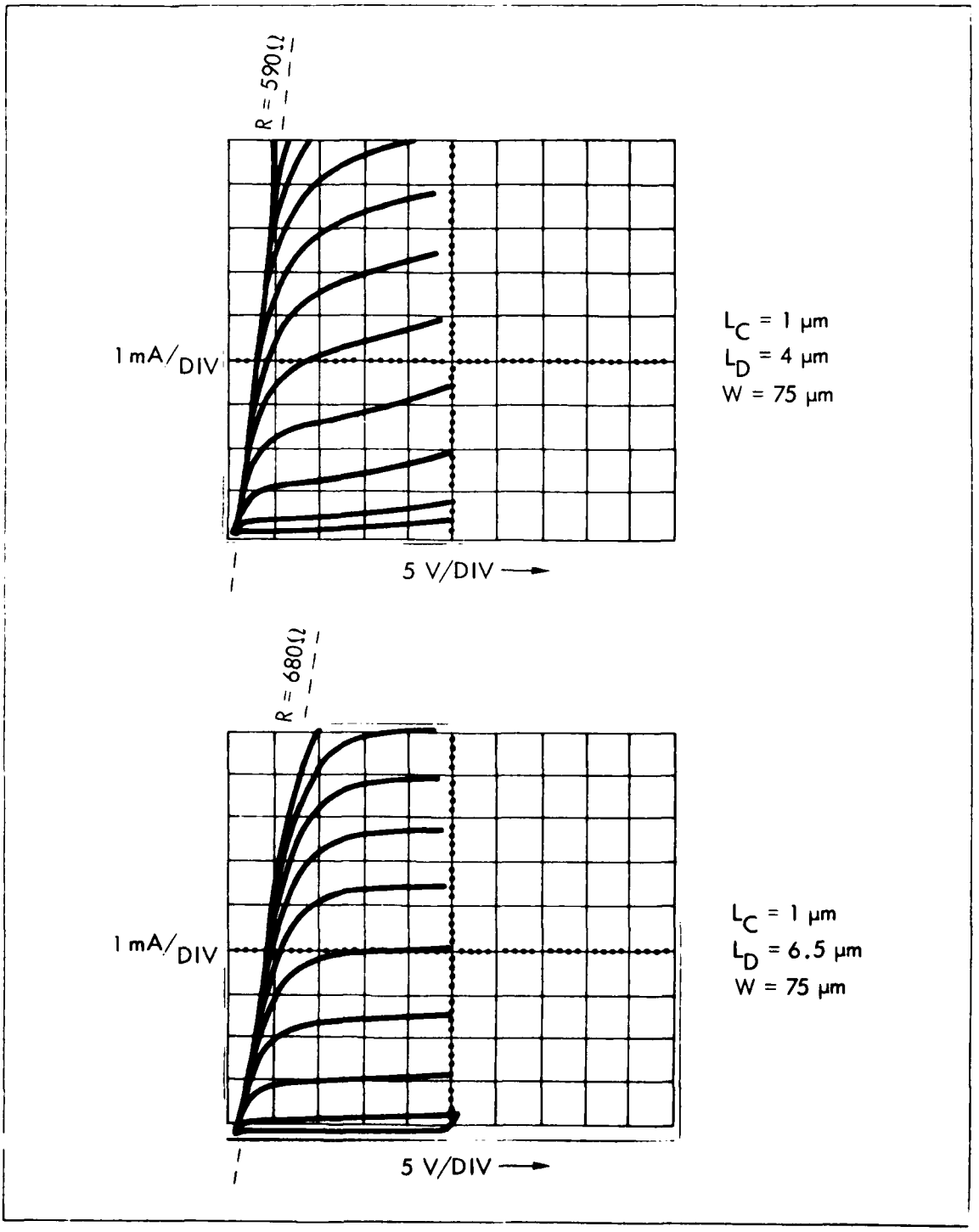


Figure 17. Source/Drain Families of ECMOS Devices (Type C) with L_D = 4 μm and 6.5 μm

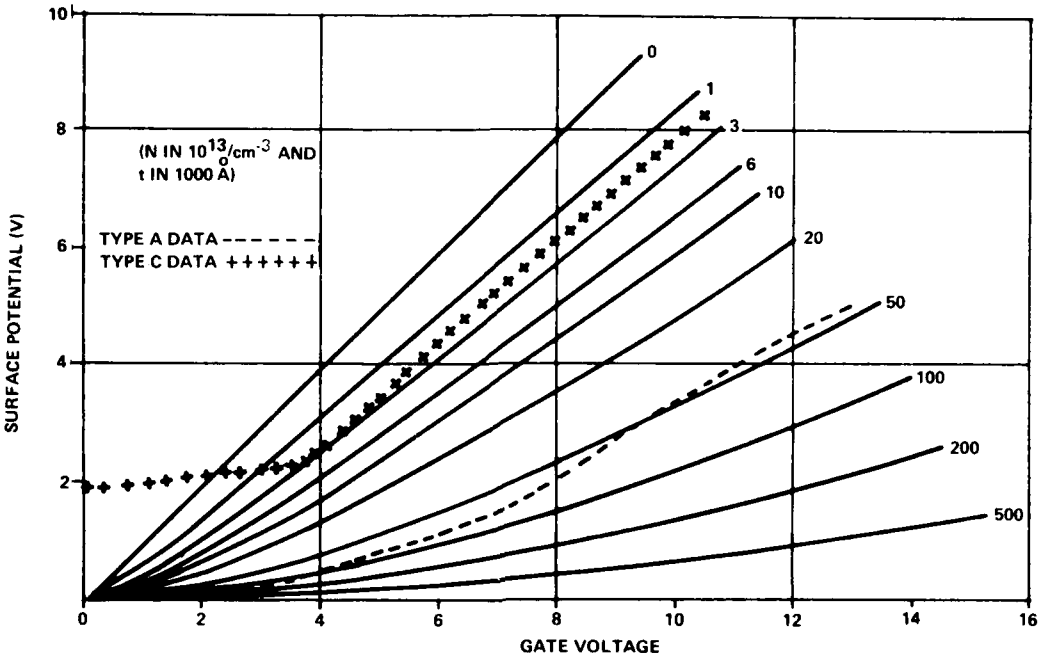


Figure 18. Gate Voltage versus Surface Potential with Nt^2 as a Parameter

5) ECMOS technology will be used for CCD input and output stages to achieve the performance of micron and submicron active channels without loss of charge handling capacity.

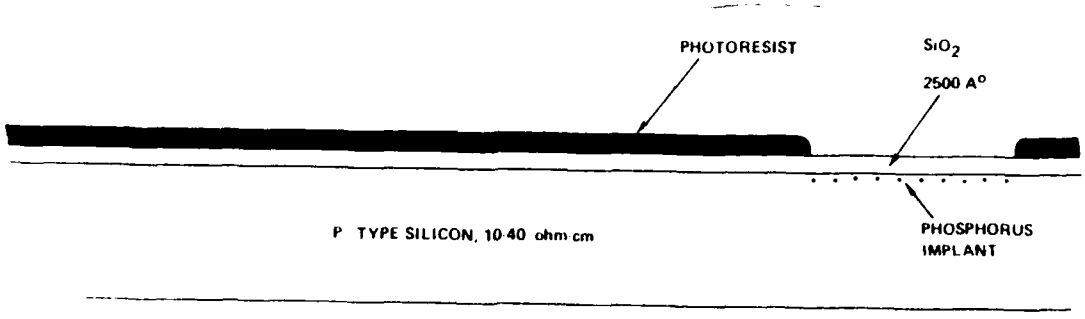
6) The substrate will be gettered by a BF_2 implant on the back, which also will provide a good back (substrate) contact.

7) Polysilicon-aluminum or Tiw-Al metallization will be used to provide uniform step coverage and reliable contact to very shallow junctions.

8) Mixed coplanar and guard band isolation will be used to optimize the performance and ease of fabrication of the CCD delay line and I/O regions and peripheral transistor circuitry.

9) Ultraclean wafer fabrication processing will be used, including the use of polysilicon furnace tubes cleaned with HCl and tight control over the quality of doping and gas supplies.

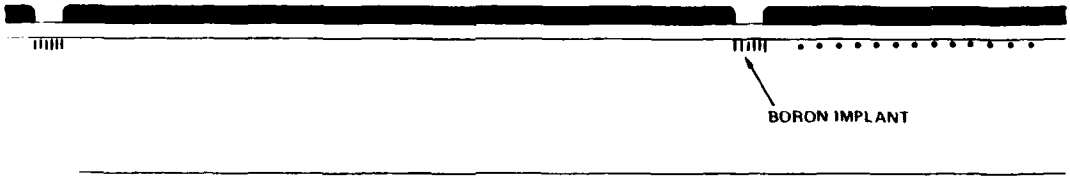
Figures 19 through 25 show the processing sequence that will be used. Since the ECMOS transistors used for peripheral circuits may see some treatments different from the ECMOS input and output sections to achieve high current amplifiers, switches, and depletion load devices, a transistor representing an output amplifier stage is shown separately in the figures.



(1) GROW 2500 A° SiO_2

(2) APPLY PHOTORESIST MASK & IMPLANT PHOSPHORUS INTO AMPLIFIER ECMOS AREA

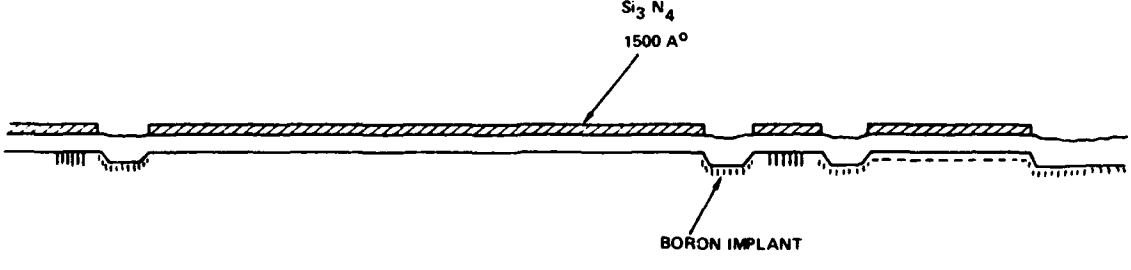
Figure 19. Steps 1 and 2 of CCD/ECMOS Compatible Process



(3) APPLY PHOTORESIST MASK & IMPLANT BORON INTO GUARD BAND AREA

(4) ANNEAL

Figure 20. Steps 3 and 4 of CCD/ECMOS Compatible Process

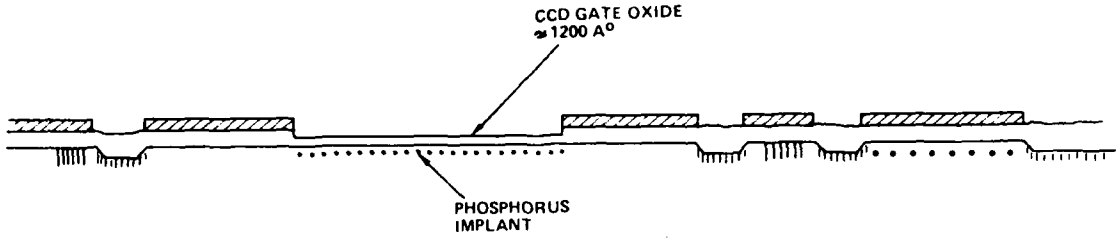


(5) APPLY Si_3N_4 MASK OVER DEVICE AREAS & ETCH BACK THE SILICON SUBSTRATE (BY ≈ 3000 A°) IN THE FIELD AREAS

(6) FORM ANTI-INVERSION LAYER BY IMPLANTING BORON INTO FIELD REGION

(7) SELECTIVELY OXIDIZE FIELD REGIONS

Figure 21. Steps 5 and 6 of CCD/ECMOS Compatible Process

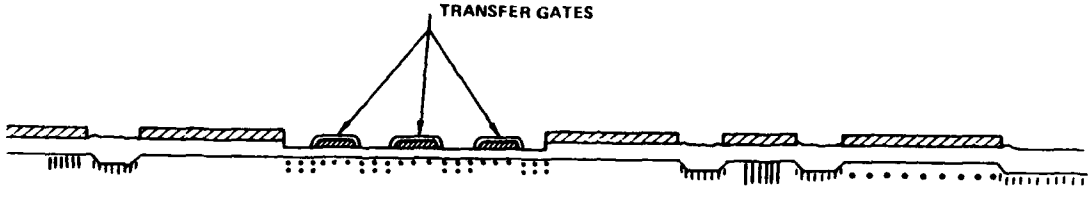


(8) REMOVE Si_3N_4 FROM CCD GATE AREA

(9) GROW CCD GATE OXIDE

(10) IMPLANT PHOSPHORUS TO FORM BURIED CHANNEL TRANSFER WELLS

Figure 22. Steps 8 through 10 of CCD/ECMOS Compatible Process



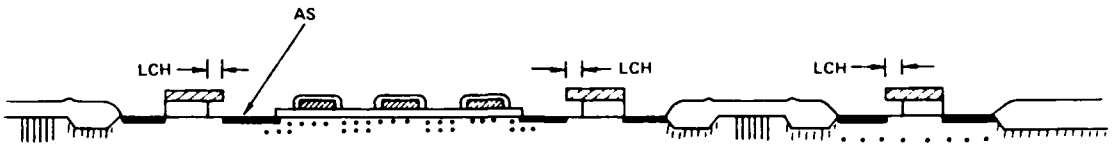
(11) DEPOSIT POLY SILICON (5000 A°)
& DOPE POLY BY PHOSPHORUS DIFFUSION

(12) DEFINE TRANSFER GATES

(13) IMPLANT ADDITIONAL PHOSPHORUS INTO CCD STORAGE REGIONS
USING TRANSFER GATES AS A MASK

(14) ANNEAL & GROW SiO_2 (≈1800 A°) ON TRANSFER GATES

Figure 23. Steps 11 through 14 of CCD/ECMOS Compatible Process



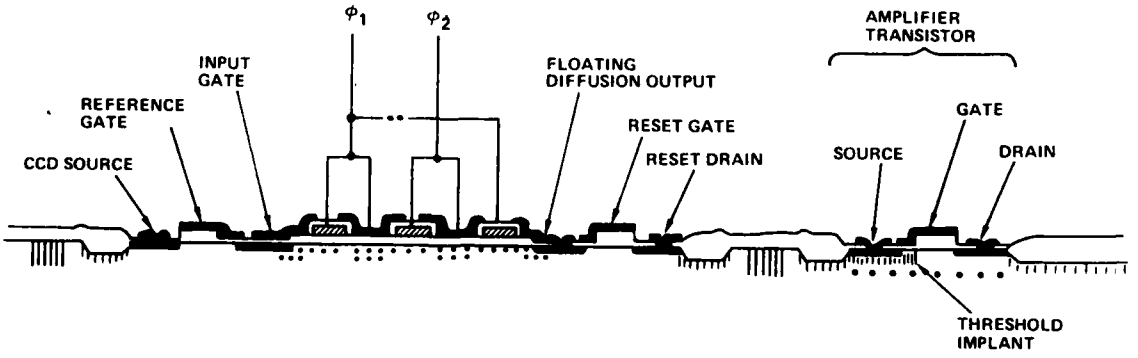
(15) REMOVE Si_3N_4 & SiO_2 FROM ECMOS SOURCE & DRAIN AREAS

(16) IMPLANT ARSENIC IN SOURCE & DRAIN AREAS

(17) ANNEAL

(18) APPLY PHOTORESIST MASK & DEFINE SHORT CHANNEL REGIONS LCH BY ETCHING BACK THE SiO_2 LAYER UNDER THE Si_3N_4 LAYER

Figure 24. Steps 15 through 18 of CCD/ECMOS Compatible Process



(19) STRIP Si_3N_4

(20) GROW GATE OXIDE FOR ECMOS STRUCTURES (700 Å)

(21) ADJUST THRESHOLD OF ECMOS STRUCTURES BY ION IMPLANT THROUGH THE GATE OXIDE USING PHOTORESIST MASK

(22) ANNEAL & DRIVE THRESHOLD IMPLANT

(23) ETCH VIA HOLES

(24) DEPOSIT & ETCH METAL GATES & INTERCONNECTS

(25) ANNEAL OUT SURFACE STATES & SINTER CONTACTS

Figure 25. Steps 19 through 25 of CCD/ECMOS Compatible Process

4. HIGH SPEED CCD/ECMOS TEST MASK SERIES DESIGN

The proposed advanced high speed CCD technology includes simultaneously fabricated high speed CCD delay lines, higher speed input/output structures and high frequency MOS transistors for both low voltage amplifier and high voltage clock driving applications.

A new mask series is being designed to evaluate various approaches to such a technology. The mask series will incorporate input/output test structures for the evaluation of conventional high performance MOS and ECMOS gate structures with a variety of channel lengths and widths. A variety of CCD designs will also be included for evaluation along with short channel MOS and ECMOS clock driver circuitry to obtain additional design tradeoff information.

Figure 26 shows the functional representation of an ECMOS input/output test structure. Note that it amounts to a high speed CCD with only a single storage well. This pattern will permit the characterization of ECMOS I/O structures for a high speed CCD without the signal degradation caused by multiple transfer and storage stages.

Figure 27 shows mask layouts prepared for the 4-1 function using channel widths of 12.5, 25, 50, 100 and 200 μm. The input and output electrodes used are of the ECMOS type and all inputs and outputs are brought to external pads so that they can be evaluated under a variety of bias and signal conditions. The purpose of this group of test patterns is to provide comparison data for five channel widths with respect to harmonic distortion noise, and transfer efficiency at both low and high operating speeds.

Figure 27 also shows the mask design for ECMOS output sample and hold and precharge transistors. These transistors will be connected to the outputs of the CCD structures with corresponding channel widths.

The remaining two structures shown in Figure 27 are ECMOS transistors with their terminals made available for individual device measurements. The smaller of the two is a minimal sized device utilizing the minimum area for the design rules used, and the larger device is the same structure extended to a 10x greater channel width.

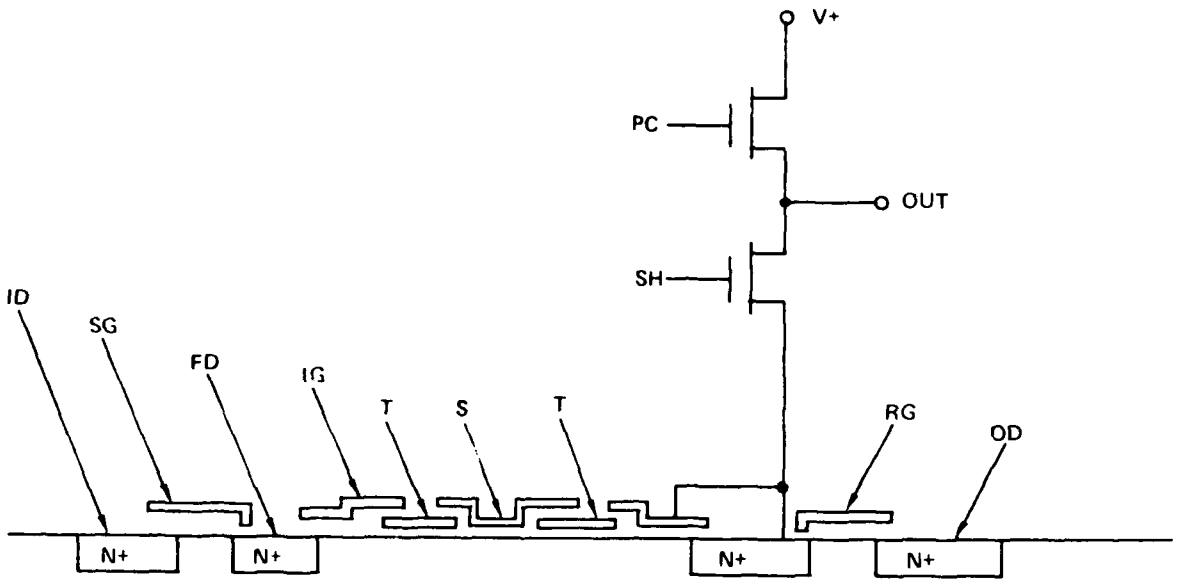


Figure 26. ECMOS Input/Output Structure Functional Diagram

Figure 28 shows the functional representation of a conventional polysilicon gate input/output test structure.

Figure 29 shows the mask design used to implement the above function using electrode lengths of 5, 10, and 40 μm and a 200 μm channel width.

Figure 29 also shows a minimum-sized and a 10x minimum channel width non-ECMOS transistor. These two transistors are self-aligned polysilicon gate devices with 5μm mil channel lengths and they will be used to compare ECMOS with conventional device characteristics.

The interconnected device pattern shown in Figure 29 is an output amplifier using the same channel widths that are used in the existing Raytheon 60 MHz CCD. Each transistor is an ECMOS transistor with much shorter effective channel widths, however. The input to the amplifier is the output of the sample and hold transistor. The test pattern will be used at a CCD output, but also be available as a separate pattern at one end of the test mask layout.

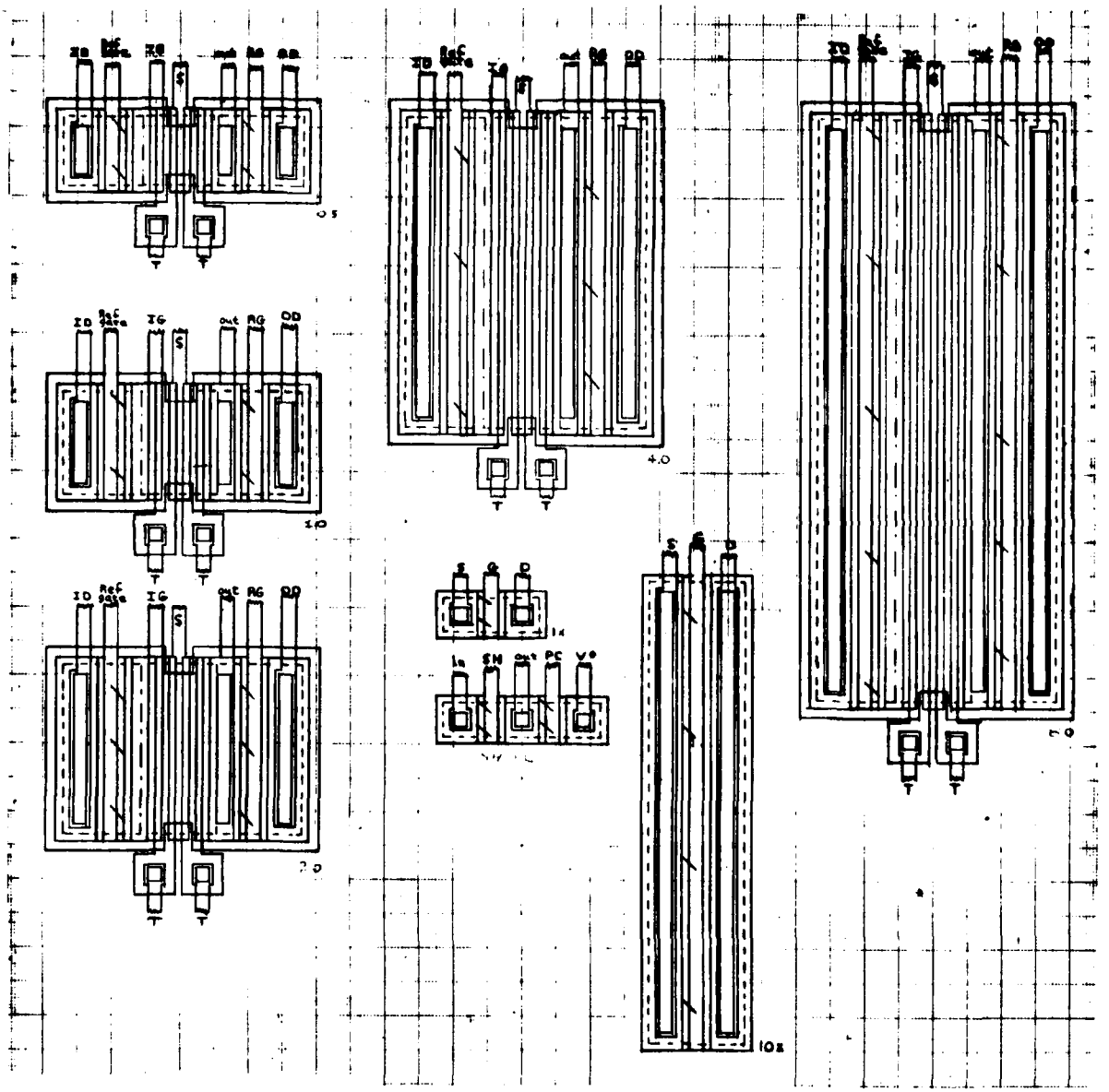


Figure 27. ECMOS Input/Output Test Structure Mask Designs for Channel Widths of 12.5, 25, 100 and 200 μm

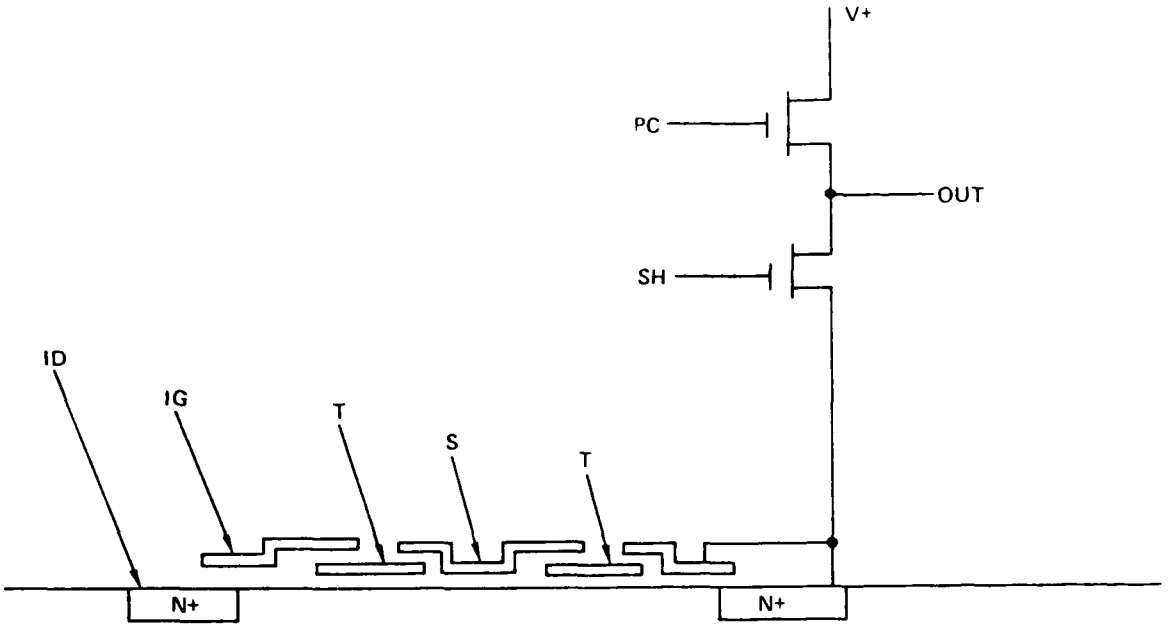


Figure 28. Conventional Input/Output Structure Functional Diagram

In addition to the test cells shown in Figures 27 and 29, the chip will contain one 256 stage CCD using ECMOS devices for I/O electrodes and output amplifier devices and a second 256 stage CCD using identical 5 μm transfer and storage electrodes but with more conventional I/O and amplifier structures. Performance of a given CCD with conventional polysilicon input/output structures will therefore be directly comparable with the performance of the same CCD using ECMOS I/O and output amplifier structures. Both 256 stage CCDs will use 50 μm wide channels and have 5 μm polysilicon transfer wells and 5 μm wide aluminum storage wells.

It is also desirable to evaluate CCD performance using storage and transfer wells that are not equal in length. In order to evaluate this option, three additional 64 stage CCD delay lines with varying lengths for transfer and storage wells will be provided for this purpose in the test mask series.

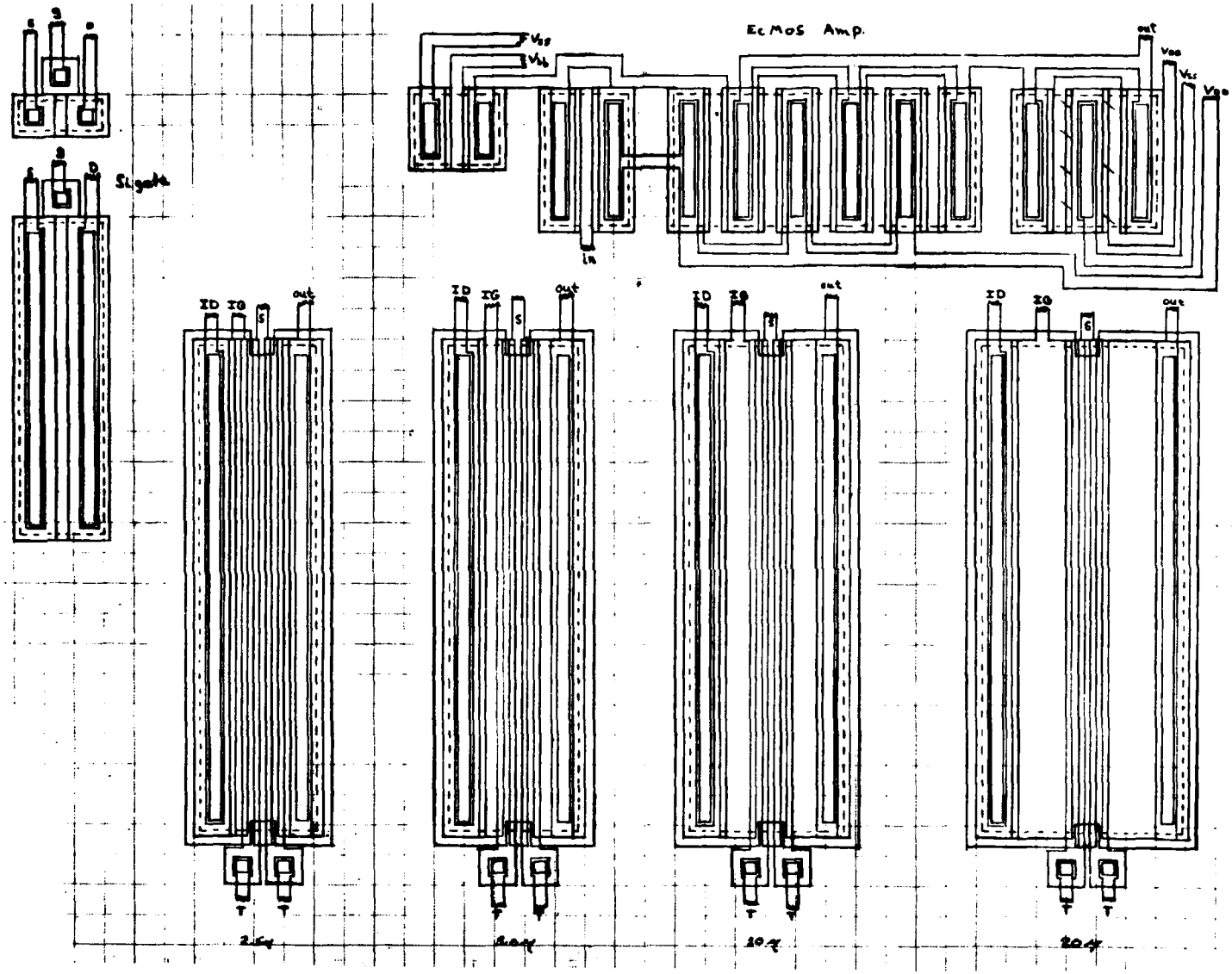


Figure 29. Mask Layout for Conventional Input/Output Test Structures and ECMOS Output Amplifier

Additional patterns will be provided in the test mask series to compare the characteristics of logic gates made with ECMOS transistors with conventional short channel NMOS transistors. Several chains of inverters will be provided with different channel widths and different load devices for this purpose.

Calculations indicate the clock lines of the 256 stage CCDs will have a capacitance of about 30 pF. Operation of these clock lines at hundreds of megahertz will require 10 V pulses with subnanosecond rise and fall times and peak currents in the order of an ampere. Delivery of clock voltages meeting these requirements will necessitate "on" resistances of the driving transistors that are no greater than a few ohms.

Figure 30 shows the expandable cell design for an interdigitated ECMOS transistor for clock driving applications. This transistor can be expanded in both the x and y direction to obtain the required channel width. Source, drain and gate electrodes are all interconnected with aluminum to obtain the low "on" resistance and fast response required for high speed/high current operation.

Delivery of clock line currents in the order of an ampere at 10 V at $fc \geq 100$ MHz will also produce power dissipation in the driver transistors in the order of 10 W. Continuous operation of these devices at frequencies in the 100 MHz and above region will require special IC packaging with heat sinking adequate for the application.

Figure 31 shows the push pull driver circuit configuration as proposed for use as an on-chip high speed clock driver. Transistors Q_1 and resistor R_1 serve to invert the input signal such that the source follower Q_2 and the sink transistor Q_3 are not "on" simultaneously. The resistor R_1 serves as the load device for Q_1 and as the source resistance when the gate capacitance of Q_2 is being charged. R_1 is often replaced with a separate MOS transistor. However, in this particular case, the N+ polysilicon 40 $\Omega/\square$ sheet resistance will provide a minimal area low capacitance "pull-up" resistor.

The Raycap computer aided design program will be used to optimize the ratios of transistors Q_1, Q_2 and Q_3 and the value of R_1 in order to achieve the maximum speed with minimum current "spiking" from the clock voltage power supply.

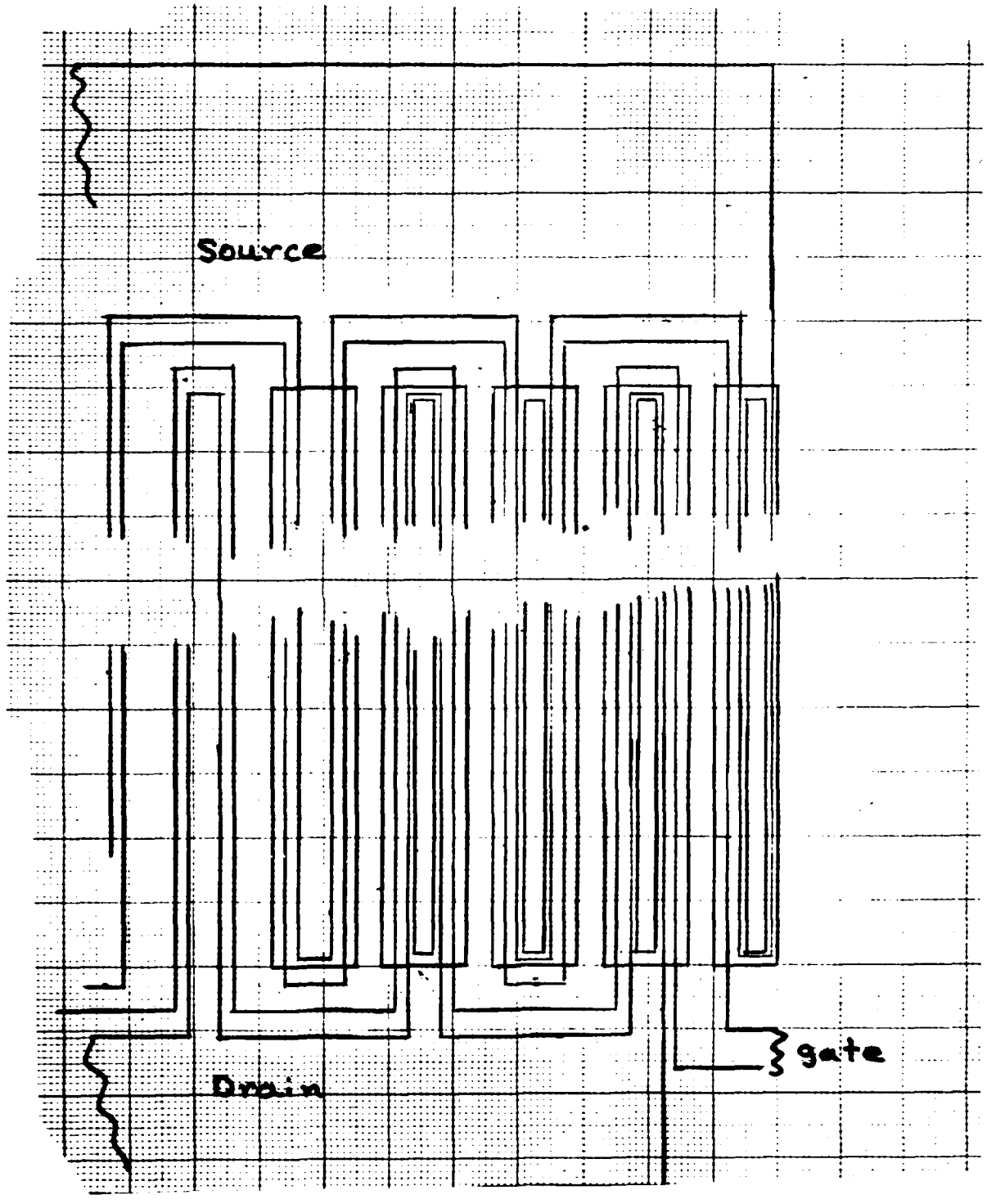


Figure 30. Mask Layout for ECMOS Clock Driver Transistor Geometry

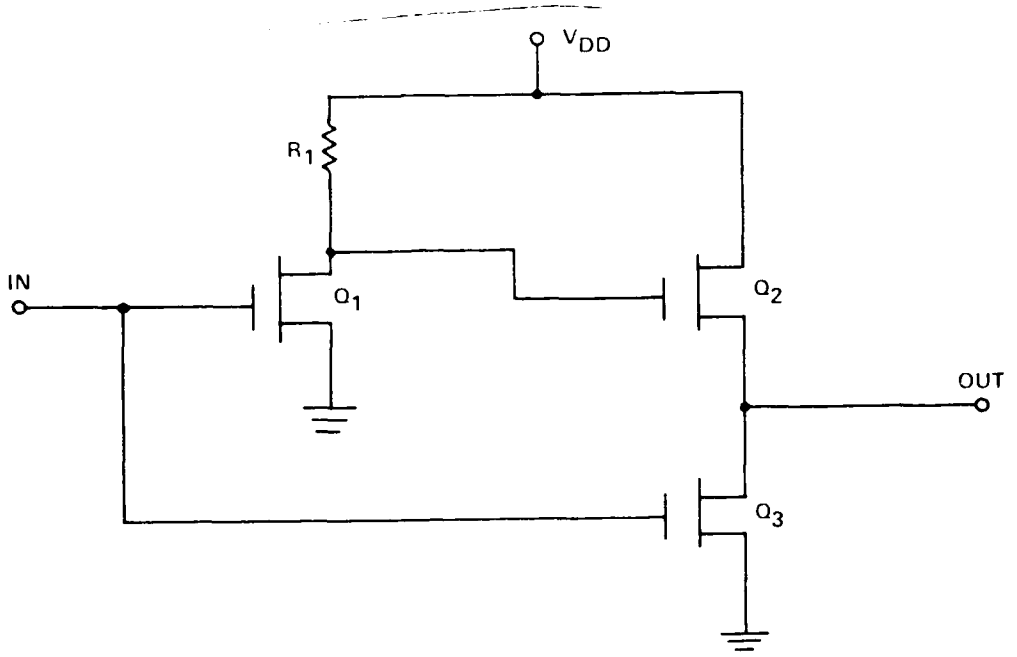


Figure 31. High Speed CCD On-Chip Clock Driver Circuit

The circuit shown in Figure 31 will also be implemented in the test chip mask design using high speed/high voltage MOS transistors.

Both ECMOS and MOS versions of the clock driver circuits will be integrated on-chip such that optional aluminum masks can be used to evaluate the CCDs and clock drivers separately or as combined integrated circuits.

Figure 32 is a plan of the completed test chip. Although not to scale, it shows the expected locations of the test patterns to be included. The two 256 stage CCDs, one with ECMOS I/O and clock drivers and one with conventional MOS I/O and clock drivers, will be in parallel with each other and determine the overall chip length of approximately 5.8 mm.

The three 64 stage CCDs with different ratios of storage to transfer cell lengths will be placed in a line in parallel with the two 256 stage CCDs. Other test patterns, including the I/O test structures, will occupy the remaining space as shown in Figure 32.

The completed test chip is expected to be approximately 5.8 mm x 2.0 mm in size.

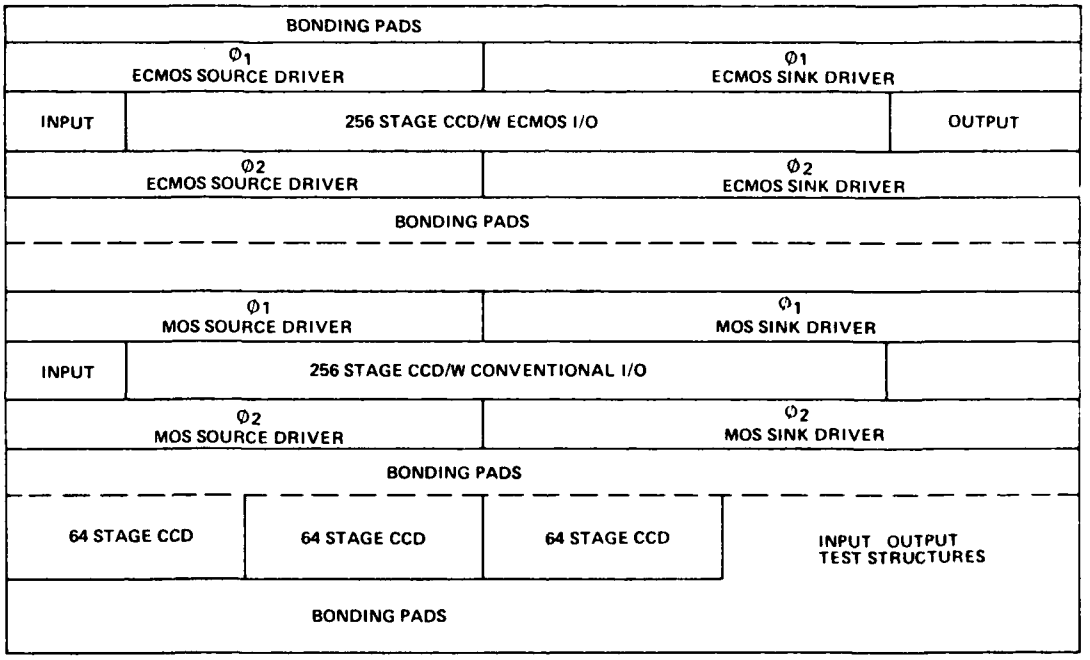


Figure 32. Chip Plan for High Speed CCD Test Pattern

5. PLANS FOR THE NEXT REPORTING PERIOD

The computer analysis of high speed CCD I/O performance will be continued. The following will be investigated using computer models:

1) Improved ECMOS potential equilibration method
2) Injection input method using MOS and ECMOS structures
3) Diode cutoff input method
4) Floating diffusion output with MOS and ECMOS structures

The design of the test mask series will be completed, masks will be generated and wafer fabrication will begin.

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